MIL-EMBEDDED.COM

HMI development requires creativity page 14

Military EMBEDDED SYSTEMS

VOLUME 4 NUMBER 6
SEPTEMBER 2008

INCLUDING:

MIL/COTS DIGEST
Small Form Factors supplement

Chris A. Ciufo
Intel *still* Inside

Duncan Young
8640D powers on

John Wemekamp
Network security

Guest Column
Safely migrating software

FPGAs do DSP for SDR

PRSRT STD
U.S. POSTAGE
PAID
OpenSystems Media/
OpenSystems Publishing

16872 E AVENUE OF THE FOUNTAINS, STE. 203, FOUNTAIN HILLS, AZ 85268

OpenSystems Media/
OpenSystems Publishing

Also:
An exclusive interview with JPEO JTRS

Solutions for Contact centers, Conferencing, Fax technology, Military applications...

Military commanders must always feel secure with their communications systems... DO YOU?

Our expertise

Aculab has become a center of excellence for many agencies delivering network centric communications solutions for deployment in tactical and infrastructure networks throughout the defense technology sector. Our advanced enabling technologies and responsive commitment to bespoke engineering development provide essential interoperability and highly effective, redundant, reliable and scalable components that enable our partners to deliver secure applications for joint land, sea and air operations.

Our difference

When you invest in a partnership with Aculab, you get more than the highest quality media processing technology that has been optimized for your sector. Whether it's for military applications, contact centers, conferencing or fax technologies, you get the reassurance of a stable and proactive partner, offering continued support and enabling you to adapt to change before it happens.

Our technology brings you

- Reduced operating costs
- Faster time to market
- Improved margins and ROI

For further information

www.aculab.com/military
info@aculab.com
+1 781 433 6000
+44 (0) 1908 273802

aculab

The technology **driving** your success

iNNODISK®
Beyond your imagination

Top Reliability, Finest Solution

InnoDisk, the leading manufacture of industrial storage devices, provides highly reliable products for the extreme operating conditions. We also offer comprehesive solutions for embedded systems and industrial applications.

FiD 2.5" & 1.8" SATA 10000 Capacities: 8GB~128GB
Read:160MB/sec.(max.) Write: 140MB/sec.(max.)

The total solution for embedded storage

SATADOM

-40°C~+85°C Wide Temp. Available

Vertical Type
128MB~8GB
Read: 24MB/s(max.)
Write: 14MB/s(max.)

Horizontal Type
Capacities: 128MB~8GB
Read: 24MB/s(max.)
Write: 14MB/s(max.)

SSD Series

-40°C~+85°C Wide Temp. Available

2.5" SATA 6000
Capacities: 8GB~128GB
Read: 60MB/s(max.)
Write: 40MB/s(max.)

2.5" ATA 6000
Capacities: 8GB~128GB
Read: 60MB/s(max.)
Write: 40MB/s(max.)

i-DIMM Series

-40°C~+85°C Wide Temp. Available

SDRAM/DDR 1/DDR 2/DDR 3

4000 Series-EDC/iCF

-40°C~+85°C Wide Temp. Available

Vertical type 40/44pin

Horizontal type 40/44pin

iCF 4000 up to 16GB

128MB~8GB
Read: 40MB/s(max.)
Write: 20MB/s(max.)

USB EDC Series

Capacities: 256MB~2GB
Read: 17MB/s(max.)
Write: 10MB/s(max.)

Capacities: 256MB~4GB
Read: 33MB/s(max.)
Write: 22MB/s(max.)

www.innodisk.com

InnoDisk USA Corporation
43154 Christy Street Fremont, CA 94538 Tel: 510-770-9421 Email: usasales@innodisk.com

Military EMBEDDED SYSTEMS

September 2008 Volume 4 Number 6

COLUMNS

DEPARTMENTS

ON THE COVER:

This Special Ops war fighter is wearing a software-defined tactical hearing enhancement headset, developed by Silynx Communications. Deployed by USSOCOM, the headset is but one example of how reconfigurable computing – usually enabled by FPGAs and DSP – is going beyond just Software-Defined Radios. But a software-defined, open architecture remains the backbone of the DoD's JTRS. Our exclusive interview with Dennis Bauman, JPEO JTRS, underscores that the program is back on track and already fielding working hardware. See articles starting on page 26. (Image courtesy of Silynx Communications.)

WEB RESOURCES

Subscribe to the magazine or E-letter:
www.opensystems-publishing.com/subscriptions

Live industry news:
www.mil-embedded.com/news
www.opensystems-publishing.com/news/submit

Submit new products:
www.opensystems-publishing.com/np

Hardware: Simulations get *real*

Technology: FPGAs do DSP for SDR

E-CASTS

www.opensystems-publishing.com/ecast

Low-power processors in SFFs
Oct. 8, 2008 • 2 p.m. EDT
Presented by: Freescale Semiconductor, Kontron, and EuroTech

Adapting the Eclipse IDE for embedded development
Oct. 21, 2008 • 2 p.m. EDT
Presented by: Express Logic

EVENTS

Vision 2008 Embedded Linux Developers Conference
Oct. 1-3, 2008 • San Francisco, CA
www.mvista.com/vision

SDR '08 Technical Conference & Product Exposition
Oct. 26-29, 2008 • Washington, D.C.
www.sdrforum.org/SDR08

Embedded Systems Conference – Boston
Oct. 26-30, 2008 • Boston, MA
www.cmp-egevents.com/web/escb

MILCOM 2008
Nov. 17-19, 2008 • San Diego, CA
www.milcom.org

Published by: OpenSystems Publishing™

The MISSION WORKSTATION

A ruggedized multi-computer workstation for applications that demand the best.

- 4 completely independent computer systems in one 19" 6U rack mount enclosure
- Every Mission Workstation is screened to a ruggedized production acceptance test including fully powered 3G NAVMAT vibration test and environmental stress screening (ESS) test.
- Can be factory configured to be powered from DC or AC sources
- All hard drives are removable
- Temperature range of -10C to 60C
- Each of the 4 computers can be independently configured with Core 2 Dual or Core 2 Quad Intel processors
- Supports multiple operating system configurations
- Can be factory configured as 4 independent computer systems or one cluster computer
- Each individual computer has 2 PCI slots, 1 PCIx-16 slot, up to 8G RAM, 4 SATA ports, 2 Gigabit Ethernet ports, and up to 12 USB 2.0 ports

- Jacyl Technology is the OEM of the Mission Workstation, contact us for custom configurations

Jacyl Technology specializes in the design and production of custom and COTS electronic systems for severe environment applications.

JACYL TECHNOLOGY

Advancing Today's Technology into Tomorrow

www.jacyltechnology.com

Military EMBEDDED SYSTEMS

AN OPENSYSTEMS PUBLICATION

Military and Aerospace Group

- DSP-FPGA.com/E-letter
- DSP-FPGA.com Resource Guide
- Military Embedded Systems/E-letter
- Military Embedded Systems Resource Guide
- PC/104 and Small Form Factors/E-letter
- PC/104 and Small Form Factors Resource Guide
- VME and Critical Systems/E-letter

Group Editorial Director	Chris A. Ciufo cciufo@opensystems-publishing.com
Senior Editor (columns)	Terri Thorson tthorson@opensystems-publishing.com
Associate Editor	Sharon Schnakenburg sschnakenburg@opensystems-publishing.com
Assistant Editor	Robin DiPerna
New Products Editor	Cliff Witte
European Representative	Hermann Strass hstrass@opensystems-publishing.com
Senior Web Developer	Konrad Witte
Web Content Specialist	Matt Avella
Creative Director	Steph Sweet
Art Director	David Diomede
Circulation/Office Manager	Phyllis Thompson subscriptions@opensystems-publishing.com

OpenSystems Media/OpenSystems Publishing

Editorial/Production office:
16872 E. Ave of the Fountains, Ste 203, Fountain Hills, AZ 85268
Tel: 480-967-5581 ■ Fax: 480-837-6466
Website: www.opensystems-publishing.com

Publishers	John Black, Michael Hopper, Wayne Kristoff
Vice President Editorial	Rosemary Kristoff

Communications Group

Editorial Director	Joe Pavlat
Managing Editor	Anne Fisher
Technology Editor	Curt Schwaderer
European Representative	Hermann Strass
Senior Designer	Joann Toth

Embedded and Test & Analysis Group

Editorial Director	Jerry Gipper
Editorial Director	Don Dingee
Senior Associate Editor	Jennifer Hesse
Special Projects Editor	Bob Stasonis
European Representative	Hermann Strass

ISSN: Print 1557-3222

Military Embedded Systems (USPS 019-288) is published eight times a year (January/February, March/April, May, June, July/August, September, October, November/December) by OpenSystems Media/OpenSystems Publishing LLC, 30233 Jefferson Avenue, St. Clair Shores, MI 48082. Subscriptions are free to persons interested in the design or promotion of *Military Embedded Systems*. For others inside the US and Canada, subscriptions are $28/year. For 1st class delivery outside the US and Canada, subscriptions are $50/year (advance payment in US funds required).

Canada: Publication agreement number 40048627. Return address WDS, Station A PO Box 54, Windsor, ON N9A 615

POSTMASTER: Send address changes to *Military Embedded Systems*
16872 E. Ave of the Fountains, Ste 203, Fountain Hills, AZ 85268

DSP-FPGA.com · VME and Critical Systems · PC/104 and small form factors · Embedded COMPUTING DESIGN · INDUSTRIAL EMBEDDED SYSTEMS · CompactPCI and AdvancedTCA Systems

Annapolis Micro Systems

The FPGA Systems Performance Leader

WILDSTAR 5 for IBM Blade

The Perfect Blend of Processors and FPGAs

Fully Integrated into IBM Blade Management System
Abundant Power and Cooling Ensure Maximum Performance

Made in the USA

Ultimate Modularity

From 2 to 8 Virtex 5 FPGA/Memory Modules
Input / Output Modules Include:
Quad 130 MSps thru Quad 500 MSps A/D
1.5 GSps thru 2.2 GSps, Quad 600 MSps A/D
Dual 1.5 GSps thru 4.0 GSps D/A
Infiniband, 10 G Ethernet, FC4, SFPDP

Direct Seamless Connections with no Data Reduction

Between External Sensors and FPGAs
Between FPGAs and Processors over IB or 10GE Backplane
Between FPGAs and Standard Output Modules

190 Admiral Cochrane Drive, Suite 130, Annapolis, Maryland USA 21401
wfinfo@annapmicro.com (410) 841-2514 www.annapmicro.com

Industry Analysis

Crunch all you want, we'll make more CPUs

By Don Dingee

If the Apple purchase and integration of P.A. Semi goes as expected, the PWRficient has joined a long list of dead CPU technology inside a defense program somewhere near you: CDP1802, MIL-STD-1750A, Z8000, Am29000, and i80960. And Freescale is dead set on the dual-core 8641D being the last of the high-end e600 Power Architecture designs, with its focus instead on designs like the QorIQ P4080 using eight smaller e500mc cores.

These are just more signs that the shift to consumer electronics has transformed the landscape for defense computing permanently. Getting any high-end CPU in a version with a higher junction temperature is difficult, and forget about getting a state-of-the-art CPU in a rad hard version. Building parts to meet defense requirements just isn't a money-making proposition for most companies.

When I wrote about this last year, I pointed out the solution might be, in part, boutique processors such as the Raytheon MONARCH. But at least one of the supporters of that architecture – Mercury Computer Systems – ended up not going that direction for production designs. "We can only support so many processor architectures," said my source. (The MONARCH uses an R3000-like instruction set, where most Mercury efforts center on Power Architecture devices.)

However, I don't think that means the concept of a reconfigurable processor in defense circles is dead. In fact, it appears that the opposite might be true – the idea might be very alive, out of necessity.

In 1990, while I was working on an IRAD project at a major defense contractor, the engineers across the hall were working on another interesting job. They were emulating the CDP1802 instruction set with Altera MAX FPGAs, a fairly straightforward job for a simple architecture using only single-issue, in-order execution.

Processors have gotten much more complex, but with FPGA cores readily available for many processor architectures, "building" your own processor device is now feasible without all the work of emulating instruction sets. These devices won't have high-end CPU cores, but they will have enough horsepower to get the job done for most applications – and much more horsepower than things like the 1750A.

Using FPGAs delivers more benefits. With the other functionality in the FPGA, other features can be directly integrated with the processor core to innovate, save space, and improve performance. FPGAs are available in extended temperature ranges, with extended life cycles, and there are some rad hard FPGA lines available.

Two examples of companies on this not-so-beaten path include:

- CPU Tech (www.cputech.com, Pleasanton, CA) has introduced their Acalis CPU872 SoC, which they call a *field programmable multicore device.* Fabbed at IBM's Trusted Foundry, the part includes Power Architecture 440 cores, embedded DRAM, and several utility compute engines. The device also has anti-tampering and anti-reverse engineering features (really their focus), and is offered in an industrial temp range with a 10-year lifespan to select customers.
- Achronix Semiconductor (www.achronix.com, San Jose, CA) is working with BAE Systems on a rad hard FPGA using its high-performance FPGA technology. Achronix claims to have one line of current non-rad hard parts operating at near 2 GHz, and another line running near 1 GHz with a super wide -260 ºC to +130 ºC temperature range.

Ray Alderman of VITA is even on this bandwagon, calling on the audience at the 2008 Critical Embedded Systems MediaFest to "innovate outside traditional semiconductor offerings" using FPGAs in order to protect designs from CPU and other component obsolescence. Not the greatest marketing term for an initiative, but the idea is solid.

We might never see a return to the days when high-end processor vendors targeted defense markets, but as long as the FPGA players and CPU core IP providers stay in the game, there should be options. And we might see some very creative solutions rise from the ranks.

For more information, contact Don at ddingee@opensystems-publishing.com.

MIL-STD-1553/ARINC 429

WHEN RELIABILITY COUNTS...

Four decades of time-proven ***reliability***, thousands of design-ins, and long life cycle support, make DDC the one MIL-STD-1553 and ARINC 429 company you can rely on for generations to come.

PMC Family

USB Family

cPCI Family

PC/104-*PLUS* Family

Toll Free: 1-800-DDC-5757

DDC®
®Data Device Corporation

www.ddc-web.com

Mil Tech Insider

Optical fiber connectivity for rugged, embedded systems

By John Wemekamp

Optical fiber is the transmission medium of choice for many military and aerospace applications because of its immunity to EMI, its lack of detectable electromagnetic emissions, its lower weight than copper cabling, and its ability to transmit high-speed signals over greater distances than equivalent copper connections. This makes it ideal for use as a secure, reliable intra-platform bus (Ethernet or Fibre Channel) or for the long-distance transmission of ultra-secure data. It has been widely adopted in commercial applications and also in less rugged military systems such as Naval combat systems and many fixed C4I installations such as battle command and air defense systems. However, the more widespread adoption of optical fiber within rugged, embedded applications has been inhibited by its incompatibility with some established embedded computing equipment, such as VMEbus and CompactPCI, resulting in suboptimal connectivity solutions.

The most rugged embedded computing applications are to be found in avionics (combat aircraft, helicopters, and missiles) and ground vehicles (tracked and wheeled armored vehicles). These two application spaces have similar requirements for packaging wherein space, weight, and power are at a premium plus conduction cooling is required to withstand the harsh environment. The military avionics market has seen the widespread adoption of the ARINC 404A ATR chassis standard, providing an ideal package size for 3U and 6U VME, CompactPCI, and VPX-based products. Maintenance procedures encourage backplane-only interconnection of modules within a chassis to prevent damage to loose cables and to prevent signals from incorrect rerouting after maintenance. Newer platforms are being designed for 2 level maintenance with Line Replaceable Modules (LRMs), which, while not constrained by ATR's limited dimensions, still cannot tolerate loose cables being plugged into the front panels.

Many interconnect solutions exist for optical fiber connection through a module's front panel. These are in widespread use in telecommunications and commercial applications. There are also many military specification (MIL-C-38999 type) optical panel connectors that can be fitted to the front of ATR boxes. However, none of these were designed for backplane connectivity in such a limited envelope space. An effective optical backplane connector must engage and disengage without the use of special tools or locking/unlocking devices, must provide very accurate alignment of fibers, and must work reliably in high-vibration military environments. Finally, in the confined space of an ATR box, the fibers must be routed from the rear of the backplane to their point of external connection without exceeding their minimum bend radius so as to not compromise signal or physical integrity of the fiber.

In order to resolve these issues and to provide a set of backplane standards for use with VPX, industry leaders, including Curtiss-Wright Controls Embedded Computing (CWCEC), are proposing a new standard, designated VITA 46.12. The standard is based on off-the-shelf fiber connector types that could be integrated with existing VPX backplane and module specifications. Three connector types, each with multiple independent vendors, are being evaluated:

- ***Mechanical Transfer (MT) –*** The MT type uses a self-aligning pair of mating shells and pins to maintain positional accuracy of fibers in the form of a ribbon cable. MT is an established commercial standard offering high connection density, but it needs care to maintain cleanliness and does not provide specific alignment of individual fibers. Figure 1 illustrates the concept of using an MT connector between a VPX module and backplane.

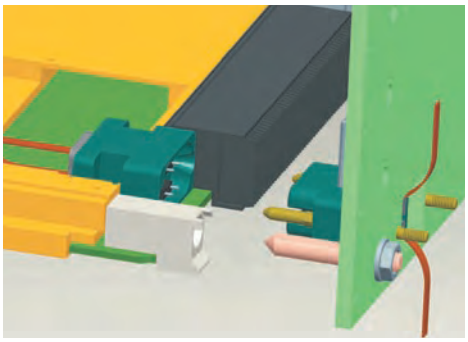


Figure 1

- ***Expanded Beam (EB) –*** This uses a spherical lens at the end of each fiber to expand the beam to many times its size. Connection is made by bringing the two lenses into close proximity without physical contact. EB connectors are less sensitive to alignment or contamination and can tolerate many mating cycles without degradation.
- ***LuxCis-type of connectors designed for ARINC 801 aerospace applications –*** These consist of metal shell pairs containing multiple signal connections using ceramic ferrules for fiber alignment, maintaining positional accuracy in high-vibration environments.

Fiber connectivity through the backplane has been an omission from embedded computing standards for too long. VITA 46.12 is supported by a broadly based industry working group of board vendors, end users, and connector vendors. It aims to develop a set of optimal connector choices based on established types supported by the results of further environmental testing. The VPX (VITA 46) standard is already proving a worthy successor to VMEbus, demonstrating its leadership by providing the first rugged, embedded computing standard for the practical use of fiber through the backplane.

To learn more, e-mail John at john.wemekamp@curtisswright.com.

ACROMAG FPGA I/O SOLUTIONS

Simply Powerful. Powerfully Simple.

VIRTEX™ 5

High-performance FPGA I/O designed for faster and easier development.

Only Acromag gives you a reconfigurable FPGA wrapped with just the features you need for fast and easy implementation. These PMC modules provide a high-speed I/O interface with plenty of memory for efficient data handling.

- Virtex-5 FPGAs (VLX155T/110T/85T or VSX95T) are optimized for logic or DSP
- Two banks of high speed 32M x 16-bit DDR2 SDRAM handle high volumes of data
- Two banks of 256K x 32-bit dual-port SRAM optimize DMA transfer to the bus
- PCI-X 133MHz 64-bit interface ensures fast data throughput
- Engineering Design Kit speeds development of custom FPGA applications.

Plug-in I/O cards extend the I/O capabilities

AXM I/O extension modules expand interface support for a wide variety of analog and digital I/O signals.

Affordable FPGA-based I/O for all your projects

Acromag's full line of industry pack and PMC modules feature Xilinx FPGAs at a range of price and performance points. Why settle for generic I/O when you can cost-effectively design just what you need?

For details on the fastest and easiest way to develop FPGA I/O visit **AcromagEmbedded.com, or call 1-877-295-7088**

Acromag®
THE LEADER IN INDUSTRIAL I/O

acromagembedded.com • solutions@acromag.com • 877-295-7088 or 248-295-0310

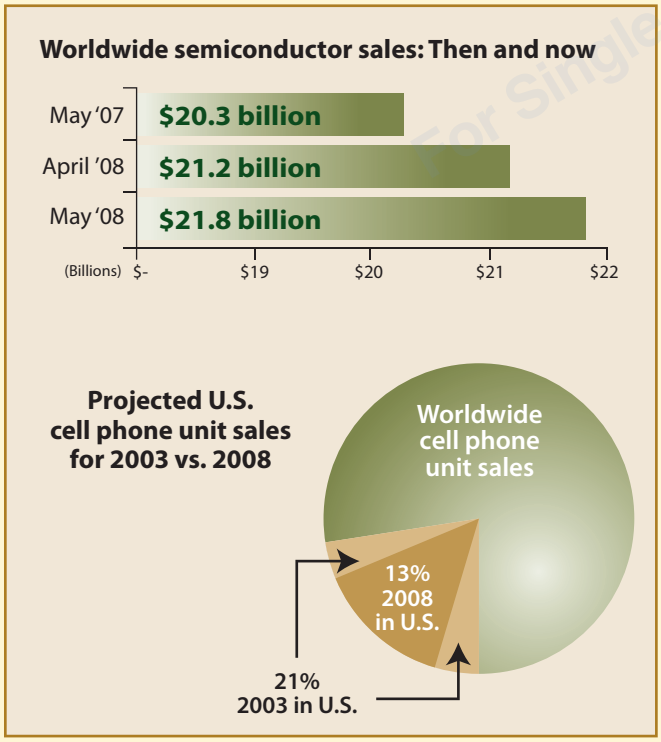
Daily Briefing: News Snippets

By Sharon Schnakenburg, Associate Editor

www.mil-embedded.com/dailybriefing

Semiconductor sales: Against the economic trend?

While the U.S. dollar continues to struggle, the worldwide semiconductor market *isn't* facing the same challenges, according to a recently released Semiconductor Industry Association (SIA) report. Findings indicate that worldwide semiconductor sales were at $21.8 billion in May 2008, a 7.5 percent rise from the $20.3 billion of May 2007. Meanwhile, May 2008 sales showed a 2.8 percent increase over the $21.2 billion of April 2008. "Despite reports of declining consumer confidence in the U.S., both disposable income and consumer spending rose in May. It is likely that the distribution of tax rebate checks to millions of Americans was a factor in increased consumer spending," says George Scalise, SIA president. The report also states that "until recently" about 31 percent of sales of PC units were U.S. based, but that today's emerging consumer markets leave the U.S. accounting for only 21 percent at present. Additionally, SIA predicts that in 2008, the U.S. will account for only 13 percent of cell phone unit sales, compared to 21 percent five years ago.



Mission computer finds refuge

… or helps those on the battlefield seeking shelter, anyway. Accordingly, Smiths Detection, provider of Chemical Biological Protective Shelters (CBPSs), recently granted a through-2016 IDIQ contract to Parvus to provide its DuraCOR 810 mission computers for Smiths' highly mobile, contamination-free shelters. The shelters are built to protect combat service support personnel and medical combat services, and the COTS DuraCOR 810 will serve as processor subsystem therein. The rugged COTS DuraCOR 810 is deployed in several manned and unmanned aircraft, naval installations, and ground vehicles. It also meets the harsh environment requirements of MIL-STD-810F and the voltage/power surge requirements of MIL-STD-1275D and -704E.

Bradley Combat System gets new SoC

Production kits for the battle-ready and -proven Bradley Combat System will soon feature the Acalis Multicore System-on-Chip (SoC). Chosen by BAE Ground Systems, CPU Technology, Inc.'s Acalis CPU420 field-programmable SoCs are low-power, highly integrated units configurable to system requirements. The SoCs contain several processors, controllers, interfaces, memories, and critical functions while reducing board count. Acalis CPU420 is scheduled for a 19-month delivery span.

New avionics safety groups take flight

Commercial airplanes and select military aircraft aren't the only ones flying in DO-178B (software) and DO-254 (hardware) avionics safety-standard style. Now two new industry groups, the DO-254 Industry Group and the DO-178 Industry Group, are ascending into the world of engineering – and looking for members. The groups are designed to provide a central repository and serve as a router to fill avionics sector needs and "energize and synergize avionics development." The groups unite vendors, developers, service companies, and tool providers in providing products, white papers, and training. Both nonprofit groups also have their own blogs at www.do178blog.com and www.do254blog.com. For more information, visit www.do178site.com or www.do254site.com.

U.S. Navy selects GeneSiC – again

Perhaps the U.S. Navy can't get enough of a good thing – or at least not enough of the Silicon Carbide (SiC) devices offered by GeneSiC Semiconductor Inc. Consequently, the U.S. Navy's Naval Surface Warfare Center, which chose GeneSiC for its Phase I SBIR project, has now chosen the vendor for *Phase II* SBIR. The project centers on multi-kV SiC device development for both power distribution systems and power conditioning within modern and legacy ship bus infrastructures. And there's more … the Navy's Space and Naval Warfare Systems Command (SPAWAR) also granted GeneSiC its Phase I SBIR award, which focuses on novel SiC device fabrication and design for high-power, high-frequency radar applications.

PikeOS is a 'GO for the DIANA project

SYSGO was recently chosen to supply its PikeOS virtualization RTOS platform for the European DIANA (Distributed, equipment Independent environment for Advanced AvioNics Applications) project. Led by Skysoft and funded by the European Commission's 6th Framework Programme, the DIANA project's goal is defining an "advanced" AIDA (Architecture for Independent Distributed Avionics) platform to support object-oriented applications' execution over secure distribution services and virtual machines. PikeOS, an ARINC-653 and MILS-compliant RTOS, will support AIDA's Flight Management System (FMS) test application.

U.S. Army sends signals

The U.S. Army recently enlisted Rohde & Schwarz's R&S SMB100M signal generators for duty. The contract between the two entities was initiated by the U.S. Army Aviation & Missile Command at Redstone Arsenal, AL. The agreement stipulates that Rohde & Schwarz provide 4,000 of its high-performance RF signal generators, along with optional support and service for seven years. The signal generators will be used for the Army's Test Equipment Modernization (TEMOD) program, which facilitates the replacement of obsolete general-purpose test equipment with off-the-shelf, state-of-the-art products. TEMOD's goal is to improve Army weapon systems readiness, reduce field equipment amounts, and cut costs of operations and support. The R&S SMB100M is a spin-off of the commercially available analog signal generator R&S SMB100A, which features a measurement range from 9 KHz to 6 GHz.

Do you see what I see?

Quantum3D Inc. recently got into the picture after QuantaDyn selected Q3D's Independence IDX 4000 Image Generator (IG) to provide upgrades to the U.S. Air Force's KC-135 Boom Operator Weapons System Trainer (BOWST). The BOWST training system helps prepare boom operators for service on the KC-135 Stratotanker, which provides in-flight refueling for Navy, Marine, Air Force, and allied nations' aircraft. Independence IDX 4000 will provide reflections on a 3D ocean, dynamic shadows, advanced weather effects, real-time lighting, alias elimination, and 8,192-pixel by 8,192-pixel shadow masks for BOWST as a result of Randolph Air Force Base's original request for upgrades. The upgraded BOWST's next stop is Altus Air Force Base.

Image courtesy of Quantum3D Inc.

Helicopter HMIs: Managing risk with automatic code generation, standards, and simulation

By Robert Kopersiewich

Photo courtesy of the U.S. Navy by Mass Communication Specialist Seaman Vincent J. Street

As helicopter Human Machine Interfaces (HMIs) continue to evolve in complexity, coding errors, project overruns, and design flaws become more of a risk. To mitigate these challenges, avionics developers can tap into useful features – such as automatic code generation, support for industry standards, and simulation – provided by COTS suppliers.

Helicopter Human Machine Interfaces (HMIs) have changed dramatically since the first turbine helicopters, the Ka-225 and a modified Navy HTK-1, were introduced more than 50 years ago. What was initially comprised of mechanical fuel gauges and altimeters has been replaced with an integrated flight data system of computers and multifunction displays that provides the pilot with key navigational, weather, and other crucial flight information (Figure 1). Today, helicopter avionics continue to evolve at a rapid pace, increasing the complexity of their development.

Integrating next-generation displays and new information sources into pilot-friendly HMIs is not the only challenge faced by avionics developers today. Developers must also manage the project and consider development costs. When the turbine helicopter was introduced, only 5 percent of its cost was for avionics. Today, avionics account for approximately 60 percent of the aircraft costs.

Now that HMI development is more complex and costly, there is a greater risk of coding errors, project overruns, and design flaws. But with a little advanced planning and the right tools, helicopter developers can stay ahead of the curve and provide customers with the most user-friendly, sophisticated HMI possible without incurring huge development costs and risks. Advances in COTS software are providing avionics developers the opportunity to take advantage of software tools that automate processes, support industry standards, and provide a platform for effectively testing the design before it is deployed in the cockpit.

Reduce risks with automatic code generation

To save time and reduce the risk of project overruns, designers should pay close attention to how they approach low-level requirements, which indicate how to write the software at the coding level without any further instruction necessary. Examples of low-level testing include the coding of objects and logic. While these features can be manually developed, hand coding requires manual bug fixing and

Figure 1

optimization, which can consume a lot of time at the project's outset. By using software with automatic code generation, low-level requirements are captured in the software's model and low-level testing is virtually eliminated. While high-level testing is still required, it is generally reduced because the code has been automatically generated and required little or no low-level testing. As the displays are created using a modeling tool, requirements are captured in early prototypes and reviews are completed early on. This can further reduce the need for high-level testing.

As the HMI moves from prototyping into production, developers must take extra care to reduce coding errors. Hand coding by nature can be unpredictable and might generate unexpected results and bugs with each iteration. Automatic code generation helps to avoid the revision of millions of lines of code when changes are made to a display – even late in the project or during the testing phase – by providing a repeatable process with a predictable outcome. For example, creating a simple blue box with a specific size using hand coding could be done in hundreds or even thousands of different ways. This increases the risk of error with the number of variations in code used across the project. To mitigate this risk, the automatic code generator will always generate the same code for the blue box in exactly the same manner, no matter how many times it is repeated.

Choosing to use tools with automatic code generation at the beginning of the project is crucial and will ultimately enhance productivity during the development process. With mandatory, safety-critical standards like DO-178B taking center stage in avionics certification, the ability to track and document HMI development is critical. The FAA requires that developers provide lengthy documentation tracking software development as part of the certification application process. This documentation can be manually created, but a code generator that is qualifiable to DO-178B comes with many certification documents and test cases to show that the HMI has already undergone significant testing to the levels required by the FAA. When a customer leverages automatic code generators qualifiable to DO-178B, they can take credit for much of the testing and documentation that has already been accomplished and reduce the time and cost of certification.

Cut costs with standardization

New avionics systems, display functions, and widgets combined with the management of hardware obsolescence during the lifetime of a helicopter can cause project overhead to skyrocket. To manage these costs, developers can opt to follow ARINC 661. ARINC 661 allows developers to access a standard set of widgets, which are objects such as symbols, pictures, panels, and buttons. These are the basic building blocks of a Definition File (DF) that will be displayed in an HMI. The DF contains pages or "layers," made up of different widgets that will be displayed on the Cockpit

Display System (CDS). Using standardized widgets reduces the amount of time required to ramp-up on projects because it makes it very easy for a developer to understand how to develop new displays. Without a standard in place, developers have to rework the coding whenever a different combination of vendors is chosen to meet a variety of file format requirements. This standard set of preapproved building blocks gives a developer the flexibility to use systems from multiple vendors: The files follow a standard format and don't require data replication or additional coding. Finally, it is also possible to reuse large parts of a DF on a new project by modifying the visual appearance of widgets, eliminating the need to start from scratch every time.

Though it is not mandatory, industry leaders such as helicopter manufacturer AgustaWestland are benefiting from ARINC 661's guidelines. AgustaWestland selected the VAPS XT ARINC 661 module from Presagis because it allows the company to quickly develop concepts for the HMI and reduce risk by providing a future path for DO-178B certification.

Tools supporting ARINC 661 development can be used to develop the look and feel of a complete widget library without working on the actual hardware. These widgets can be created graphically, using the low-level building blocks that are provided with the tools, or through programming. Objects created through programming need to be coded from scratch using traditional software coding tools, but when they are created graphically using a modeling tool, there is no coding involved. Developers use modeling tools to select aspects such as lines, colors, and text from the user interface, and the tool automatically generates the code for the completed object. This supports quick changes to their appearance during an iterative development process without needing to modify or create a single line of code. To define behavior of objects, developers will then use state-charts, such as the one depicted in Figure 2, to select elements of the design to create triggers and actions inside the application logic. By using ARINC 661-supported software, the need to repeatedly hand code behaviors across multiple widgets is eliminated. Instead the state-chart logic can be applied to each instance of a customer object, saving time and eliminating the risk of human error.

Put the HMI to the test in a simulated environment

Before the HMI is deployed to the cockpit, it is crucial to test its functionality. No

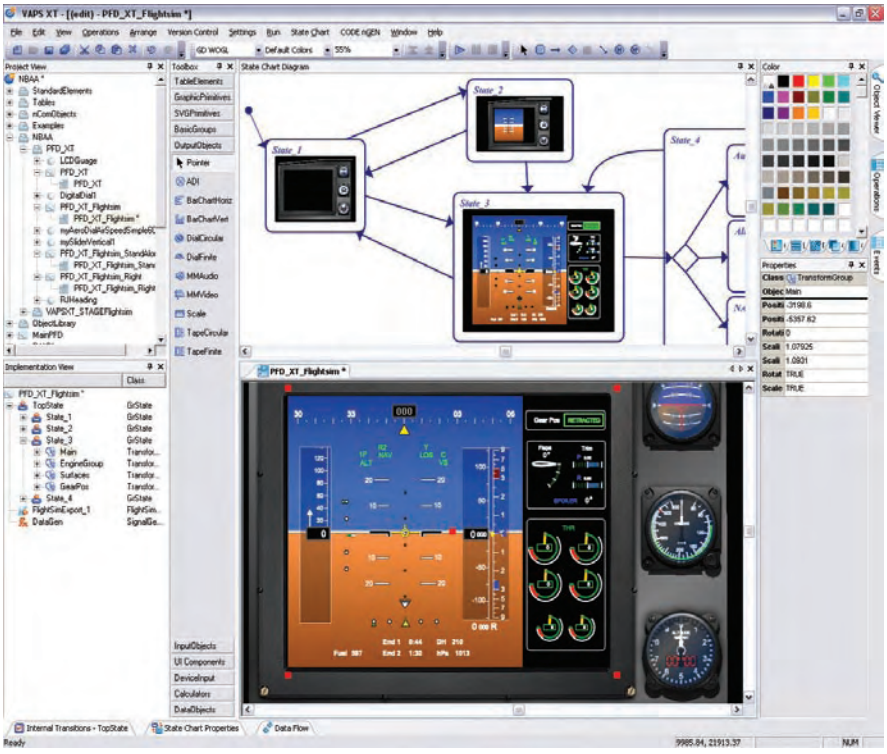


Figure 2

one wants to discover during pilot training that activating a combination of display functions in a specific sequence causes a critical system failure. No one wants to be forced back to the drawing board and have to repeat the entire development process either. Consequently, HMIs are evaluated on many criteria. For example, will the HMI allow pilots to act intuitively, helping them quickly make and execute the right decisions? In order to properly make this assessment, designers need to test the HMI in a simulated environment such as the one shown in Figure 3.

To ensure new HMIs will function as intended, they must be tested under a wide variety of conditions, such as brownouts, which occur when dust or sand in the air reduces in-flight visibility. By simulating a rich immersive environment, designers can test the HMI in a realistic 3D scenario that tests the ability of the HMI to process and present flight information. Creating a simulated environment for testing helps save money in the long run by allowing developers to see how the HMI functions before it is embedded into the cockpit. If anomalies such as alignment, usability, and performance issues are identified, an automatic code generator will become particularly handy, as it allows the developer to easily make changes and reiterate the process.

An advantage of using COTS tools for simulation and testing is that the software can be used across a multitude of platforms out-of-the-box. Avionics developers can take advantage of COTS tools to design HMIs and create the simulated environment for HMI testing. Using

Figure 3

Rugged High-Speed Data Recording and Storage

10GbEthernet
SerialFPDP
Custom

Vortex Data Recording and Playback Systems

Fibre Channel Storage Area Network

Solid State or Rotating Media

Powerful

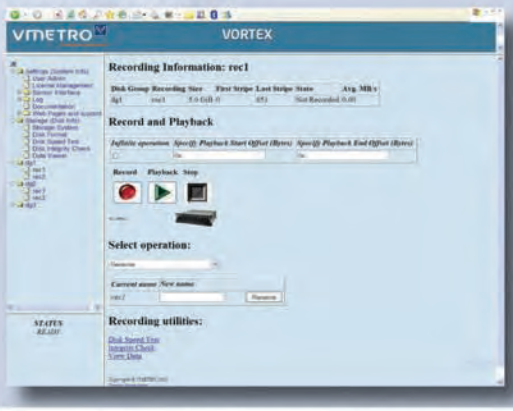
- Streaming data recording platforms with up to **720 MB/s** per recording engine sustained recording performance
- Scalable Fibre Channel SAN architecture providing virtually limitless storage capacity
- Ready-to-run application examples

Flexible

- Customer programmable or application specific recording and playback systems
- VXS (VITA 41), VME, CompactPCI and Industrial PC recording engines
- Solid state or rotating media options from rugged to commercial

Innovative

- Access and control using web browser or XML-RPC
- Disk grouping and intelligent disk management



Embedded Computing - Data Recording/Rugged Storage - Bus/Protocol Analyzers

For more information, please visit
http://www.vmetro.com/recorder
or call (281) 584-0728

VMETRO
innovation deployed

> “Using simulation at the very beginning stages of development to test prototype concepts and receive early feedback from end users, avionics developers can eliminate the risk of creating an HMI that pilots do not find intuitive.”

simulation at the very beginning stages of development to test prototype concepts and receive early feedback from end users, avionics developers can eliminate the risk of creating an HMI that pilots do not find intuitive. By leveraging a simulated environment, they can also put the final HMI through its paces and test its maximum threshold. With COTS simulation software, developers can test the HMI while the pilot flies different missions in a simulated virtual environment.

The end result: A sophisticated, pilot-friendly HMI

The helicopter cockpit has evolved from an electronic flight instrumentation system to an integrated flight data system. As a result, HMI development projects have increased in complexity, presenting unique challenges and risks, such as coding errors, project overruns, and design flaws. To mitigate these risks, avionics developers can tap into useful features – such as automatic code generation, support for industry standards, and simulation – incorporated by COTS suppliers that have broad access to the marketplace. This allows avionics developers to leverage tools that have already been proven across a wide number of systems, which means they can minimize the amount of time spent developing tools and focus on what they do best: developing effective, pilot-friendly HMIs.

Robert Kopersiewich *is vice president, product and program management, at Presagis, where he oversees and directs the growth and trajectory of the Presagis product portfolio and business road map. With more than 15 years of experience identifying and addressing key market needs, Robert plays a key role in the future success of Presagis. In 2004, he was named director of product management at Engenuity Technologies. Prior to joining Engenuity, he worked for a number of leading companies in both the telecommunications and optical-disc industries. He can be contacted at Robert.Kopersiewich@presagis.com.*

Presagis
1-800-361-6424
www.presagis.com

Digital Molecular Matter:

Realistic material damage for military training simulations using real-time Finite Element Analysis

By Steve Griffith

DoD photo by Master Sgt. Kevin J. Gruenwald, U.S. Air Force

Depicting material damage in military simulations has traditionally been a labor-intensive and expensive proposition. Now a new technology called* Digital Molecular Matter *(DMM), in conjunction with real-time Finite Element Analysis (FEA), promises to drastically improve simulation realism while reducing development time and cost.

Preparing war fighters for military engagement is both extremely important and extremely complex. The rules of engagement have changed over the years as battle lines are not always clearly defined. Today's war fighters are not trained simply to overtake the enemy. They must be aware of civilians caught in the proverbial crossfire of war. They must strive to achieve the goals defined for specific operations, minimizing any collateral damage that might come about.

Realistic training simulations depicting battlefield damage can help today's military achieve these goals, and that's where simulation designers and developers come in. They must seek out new technologies that enable the creation of more realistic simulations. They must also be agile in adapting simulations to the shifting requirements of the moment.

Demand for increasingly realistic simulations – combined with shortened development timelines – is creating tremendous challenges for military simulation designers, developers, and managers. A new technology called *Digital Molecular Matter* (DMM) uses real-time physical modeling to address these challenges, producing more realistic simulations while meeting rapid design-to-delivery requirements.

The problem with art swapping

Recent advances in simulation platform technology allow for the rendering of highly realistic scenes; however, they do nothing to improve the kinetic realism that is just as important, if not more, than the visual realism – especially in military simulations. Stated another way, objects in the simulation need to look good, but they must also move and behave as realistically as they look.

Military simulations today rely heavily on *art swaps* or real-time substitutions of art assets to deform and break objects. When a projectile strikes a concrete wall, a script is run to show the wall crumbling. To create this effect in a simulation, artists have to draw hundreds of individual frames to show the slightest bit of motion or movement.

This approach limits an object's behaviors while greatly increasing the effort and time required to develop the simulation. A breaking pane of glass, for example, will always break the same way regardless of the simulated forces acting against it. Should a simulation require a change of material, such as the addition of bullet-resistant glass, new art assets need to be created and scripted to depict the new behavior. The time required to produce art swaps to depict kinetic effects drives up the cost of simulation development and can make the cost of updating an existing simulation prohibitive.

In an effort to improve kinetic fidelity, many simulations incorporate *Rigid Body Dynamics* (RBD) systems with art swapping to generate emergent behaviors. This approach has several disadvantages. Unconstrained emergent behaviors tend to produce unintended consequences and side effects, especially as the number of interactions between objects increases. And RBD is a very limited way of representing the physical properties of simulation objects. Simulation developers using RBD have only 10 variables to describe very complex materials: 3 translations, 3 rotations, mass, inertia, dampening, and coefficient of restitution (bounciness).

If simulation developers have any hope of meeting customer expectations going forward, they need a new approach that provides greater freedom to define and describe kinetic properties.

FEA provides thousands of degrees of freedom

The most promising approach to *kinetic fidelity* is to utilize *Finite Element Analysis* (FEA) in real time. Using FEA, a solid object is divided into constituent subparts, or elements. Stresses applied to the object as a whole are interpreted as stresses to the individual elements. The result is a more granular and realistic view of how an object reacts to stress.

Offline FEA simulations have been used in the manufacturing industry for many years. FEA simulations are used to test and refine designs before the prototype phase of production – reducing the number of prototypes required, improving time-to-market, and reducing costs. Figure 1 shows how a car deforms using Finite Element Analysis.

FEA utilizes a mesh to discretize a solid object into a set of discrete elements. Calculations can then be applied to these elements to visualize where objects bend and twist and reveal the distribution of stresses and displacements. Utilized in

a real-time simulation environment, FEA allows for a vastly more realistic representation of a simulated material. Armed with FEA in real time, simulation developers have thousands of degrees of freedom in describing how each discrete element can move and interact with the simulation environment. Moreover, the properties of these elements can be set to accurately behave like real-life materials: concrete crumbles; metal bends, deforms, and tears; and wood breaks and splinters. The result is kinetic fidelity never before seen in real-time simulations.

Materials can react in entirely new ways each time the user engages in the simulation. So when a tank drives through a brick wall at different angles, the wall will crumble differently each time. What is more, art objects developed with an FEA mesh are created once, and their fracture and deformation behavior is determined by their material properties and rendered in real time – eliminating the need for art swapping.

Not only is the software advancing, but processor technology has caught up. Modern processors can now run finite element-based simulations in real time.

Using real-time FEA technology, simulation developers can vastly improve the visual and kinetic fidelity of their simulations while reducing asset creation time and cost. Simulations no longer need be scripted scenarios, and time-to-deployment is exponentially faster.

Digital Molecular Matter facilitates FEA

DMM is a real-time implementation of finite element physics. DMM technology is implemented as a real-time engine subsystem that runs independently of the primary simulation system; it also includes the tools required to convert ordinary meshes created by artists into finite element volumetric meshes.

A key advantage of DMM is the ability to add FEA effects to new objects as they are created or to existing objects for enhanced capability. With minimal effort, simulation developers can leverage their existing investments by adding DMM capability to legacy simulations.

Originally conceived by Pixelux Entertainment for the gaming industry, DMM attracted the attention of LucasArts, who wanted to deliver state-of-the-art gameplay technology in its upcoming *Star Wars* and *Indiana Jones* video games while reducing production costs. In late 2005, Pixelux began working in partnership with LucasArts to develop and refine DMM into an artist-friendly technology that could deliver the promise of finite element physics.

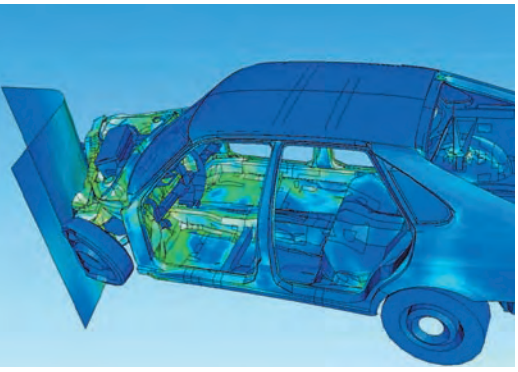


Figure 1

Figure 2

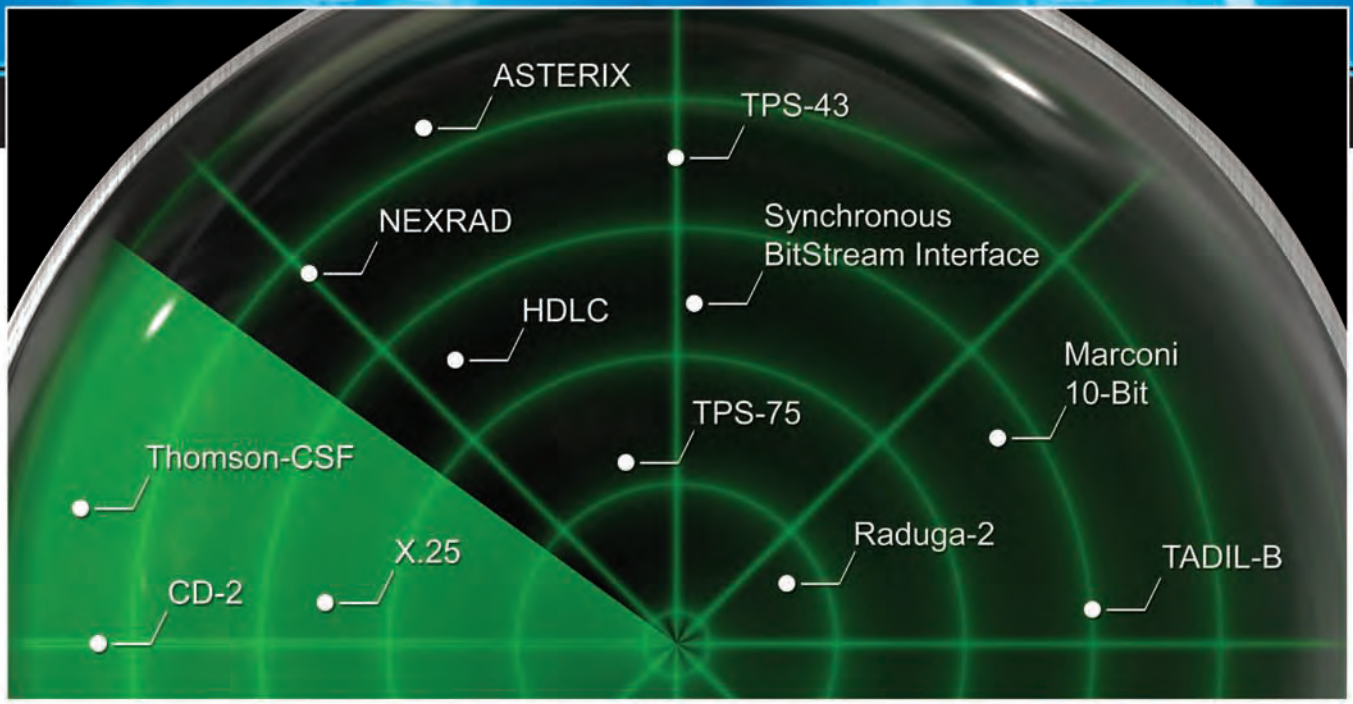
Pixelux subsequently partnered with Objective Interface Systems (OIS) to adapt DMM to the military and aerospace simulation market. The resulting product, DMMfx, was introduced at the I/ITSEC 2007 trade conference.

DMMfx provides the means to deploy military simulations with realistic deformation and fracture of materials. Wood twists, splinters, and breaks like real wood; metal deforms, bends, and tears; and glass shatters like glass. Damage such as buckling, tearing, and fracture, along with collateral effects, occur in expected ways. Simulations perform with unpredictability and realism, making them more effective. Figure 2 shows a tank breaking through wooden fences in a simulation using DMMfx.

DMM architecture and implementation

The DMM subsystem runs independently of the primary simulation engine, exchanging information about forces being applied to a scene, determining whether objects are being kinematically driven, as well as other physical interactions. Force feedback is a natural result of these interactions and can be used to generate additional visual effects and realistic sounds resulting from collisions and distortions.

The process for adding these effects is straightforward, utilizing techniques familiar to simulation artists. Artists start with a surface mesh for a new or existing object. This mesh is then used as the basis for a tetrahedral "cage." This cage is then used to create a tetrahedral mesh of the volume of the object. Finally, if the object



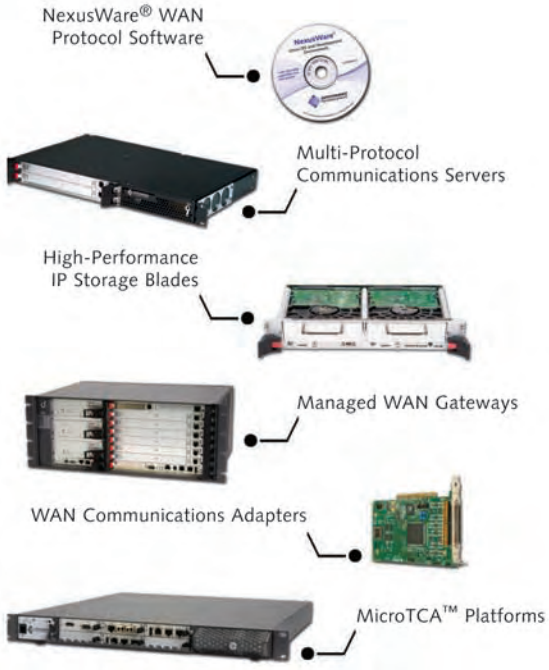
What's on your Radar?

Performance Technologies' NexusWare® WAN protocol software provides a seamless connection to a broad range of telecommunications, aerospace and defense, and commercial applications for both emerging and legacy networks.

With over 25 years experience developing highly reliable and scalable solutions, we can provide you with integrated hardware and software that can meet your product needs today and allow for future migration tomorrow.

Managed WAN Gateways, Radar Extraction, Recording Servers, and Lawful Intercept Platforms are a few of the many applications that utilize our broad software offering. Available on a suite of hardware platforms in PCI™, PCI Express®, CompactPCI®, MicroTCA™, and stand-alone form factors, our flexible WAN protocol solutions can easily accommodate a wide range of data and communication network requirements.

Explore the limitless possibilities for your programs by calling Performance Technologies today.



PERFORMANCE TECHNOLOGIES

Phone: 585.256.0200 • www.pt.com/radar5 • E-mail: info-request@pt.com

The Flash Storage Leader

Wide Temp.

-40 degree~+85 degree

- Ultra DMA Mode 6 Support
- Compliant Compact Specifications
- No Seek Error No Noise
- Low Power Consumption
- Shock Resistant & Anti-vibration
- No Latency Delay
- RoHS
- Form Factors in 1.8"/2.5"
- SATA I,SATA II, IDE and ZIF Interface
- SLC/MLC Flash IC Technology

On Sale!

PQI Corporation
Tel:(510)651-7281
Fax:(510)651-7240
For information,please contact:
dom@pqimemory.com
Learn more at: www.pqimemory.com

pqi

is breakable, the mesh has to be clipped against the surface mesh and have internal faces added that will be visible when the object breaks. Figure 3 shows a typical DMM workflow.

In addition, DMM also implements a visual enhancement called *splinter geometry.* Splinter geometry allows for the visually correct disintegration of objects that are naturally made up of component pieces such as wood, brick walls, and stone buildings. Splinter technology provides an increase in realism by fracturing objects in ways that appear more complex, without having to create a denser mesh. Figure 4 shows a timber being twisted and splintering.

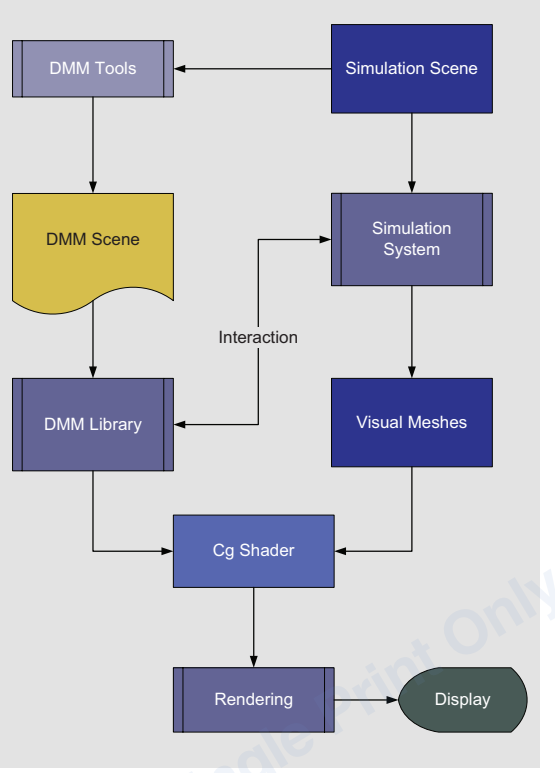


Figure 3

Figure 4

DMM also provides the ability to optimize scene performance by compressing objects within a scene, or by freezing inactive portions of a scene to relieve the system from having to simulate unused elements. Meshes not in live use are made dormant until they are needed.

Better simulations, better results

Improving military simulations to realistically depict material damage is crucial to the success of today's war fighters. Going forward, military simulation developers cannot afford to continue to rely on art swaps to depict the fracture and deformation of objects, so a new approach is needed. Improvements in simulation platform technology make the implementation of real-time Finite Element Analysis through Digital Molecular Matter a practical solution. Using this approach, military simulation managers, designers, and developers can deploy more kinetically realistic simulations while reducing development time and cost. The result is a better-trained war fighter capable of meeting the demands of the battlefield today and tomorrow – while reducing collateral damage.

Steve Griffith *is the director of business development for physical modeling and simulation at Objective Interface Systems. He has more than 20 years of business development, engineering, and management experience in the software industry. He can be contacted at steve.griffith@ois.com.*

Objective Interface Systems
703-295-6500
www.ois.com

Back on track:

JTRS JPEO assures open SCA and coalition use

EDITOR'S NOTE

Group editorial director Chris Ciufo and editor Terri Thorson conducted an exclusive interview with Dennis M. Bauman, Joint Program Executive Officer, Joint Tactical Radio System (JTRS) at the AFCEA West show in San Diego earlier this year. The key questions on their minds surrounded the progress of JTRS – which had just been essentially "rescued from the dead" after a "stop work" order had been rescinded – as well as how COTS and open architectures might benefit the many JTRS product lines. Edited excerpts follow.

MIL EMBEDDED: ***JTRS is all about interoperability between services, different waveforms, and hardware types. But how would you describe the applicability of the JTRS Software Communications Architecture (SCA) to all of your vendors – and to the greater SDR industry at large?***

BAUMAN: We think it's very open, based on our SCA and APIs. There are 26 of them currently [corresponding to the JTRS waveforms]. Those are the Increment One APIs, and we're continuing to refine them for future increments. What we do is obtain government-purpose rights on all the software developed on JTRS, and then we put it into an information repository. The repository is like a library, and we give out library cards to any industry people who want it. But they have to agree to, number one, use it for government purposes and tell us what they are using it for. Number two, if they change it, they've got to give back the changed code for the repository with government-purpose rights or better.

So JTRS is not quite as open as Linux because we have security issues that Linux doesn't, but we think we are pretty close. What we achieve by doing this is reusability and the resulting cost savings, along with interoperability because we are using the same software across all our products. This allows us to swap out vendors because we have these kinds of "Lego" building blocks in our repository. So if we aren't getting what we want from one vendor, we can buy that same module from another vendor.

MIL EMBEDDED: ***To what extent have you verified that Boeing's SCA implementation, for example, is consistent with GE Fanuc's SCA implementation?***

> "One detractor to it, though, is that we make [JTRS] so open that a lot of vendors who embed their own Intellectual Property and are dependent upon maintaining IP are a bit taken aback by how open the standard can be."

BAUMAN: We have something called the *JTEL lab*, which tests and certifies all products for SCA compliance. The lab does that through a series of automated tools that go through and look for possible discrepancies that are then flagged. Next, the lab performs manual tests and inspections to determine whether a vendor's product meets the SCA. If it doesn't, then we send specific problems back to the vendor and get them to correct them.

MIL EMBEDDED: ***So could you, API issues notwithstanding, unbolt Thales' implementation of SCA and marry it to a Boeing AMR cluster?***

BAUMAN: We're doing that already. The waveforms that are going to be used in Boeing's products are produced by a variety of vendors, for instance, ITT is under contract to do SRWs. There are multiple vendors who are under contract and are producing waveforms that are going to go on all the different boxes. That's the whole idea of the repository, and the whole operating environment on GMR was shared and used on MIDS-J [Multifunctional Information Distribution System].

MIL EMBEDDED: ***How many of the original 32 waveforms are still being ported and made SCA compliant?***

BAUMAN: I'd have to check the number, but it's between 9 and 12. But we didn't drop the others. One of the things we did in the short term was go for a "big bang" approach to JTRS, with the incremental approach. And so in Increment One, we have a subset of those original 32 waveforms, decreased down to the 9 or 12, but we also added a couple.

Anyway, everybody says we shrunk the requirement, but that's not entirely true. We shrunk it in some aspects, but we went from a single waveform networking form, WNW, to three of them in Increment One, for example. The reason is that there's a difference in number, like in UHF satcom. If you count 181, 182, 183,

and 184 as four different waveforms, then you have a different number at the end than if you count UHF satcom as one waveform.

MIL EMBEDDED: ***To what extent do you think the SCA will be adopted by the commercial market, which was one of the original pushes of the program?***

BAUMAN: I don't know. I know that it's being seriously considered for adoption by our international coalition partners. There was at one point a push in Europe to build their own SCA, and that's atrophied. You know that you could define many standards that are like the SCA (yet different), and they'd probably work just as well. But what we're trying to convince the world is, here's one that's here, so why not use it?

MIL EMBEDDED: ***Are there any definite outreach efforts to the likes of Nokia, Ericsson, or other civilian companies?***

BAUMAN: We have done that through the Software-Defined Radio Forum. Quite frankly, we're seeing a lot more traction with that in the past six months. And the reason for it is that if you compare where JTRS is now with the big downturn in the IT world, there was a big "Let's go from second-generation cellular to third-gen" push five years ago. Well, the business case in light of the downturn just wasn't there. But now you're seeing some of the third- and fourth-generation cellular products being rolled out. So there is now increased interest on the industry's part to look for more open systems standards, and we have one that's perfectly viable. One detractor to it, though, is that we make it so open that a lot of vendors who embed their own Intellectual Property and are dependent upon maintaining IP are a bit taken aback by how open the standard can be.

MIL EMBEDDED: ***To what extent do you think* any *JTRS implementation is going to utilize cognitive radio capabilities?***

BAUMAN: We consider cognitive radio to be at the forefront of technology. Well, one thing you do as an acquisition fundamental is you don't adopt technology before its time. I think cognitive radio technology is very promising: It can help us with spectrum – and in a lot of ways. But it's too leading edge to put into production at this time. We are working with DARPA on that. Actually, I believe cognitive radio is a capability cap in Implement Two that we're currently looking at. But it's not ready for prime time, and we're not putting it into Increment One as part of our requirements discipline.

MIL EMBEDDED: ***What are your plans for tech refresh?***

BAUMAN: Our plans for tech refresh will be part of Increment Two, and we will be filling capability gaps as defined by the JROC [Joint Requirements Oversight Council] as part of the requirements process. When we roll out the new capability, we intend to do technology refresh as needed in that same development to minimize future changes to our boxes' architecture and thereby preserve affordability. When you make a fundamental architecture change, there's a very long process with the NSA to make sure you don't have a vulnerability. We want to be careful that we don't require ourselves to spend more money recertifying and restudying that architecture. So we'll be doing technology refresh in terms of upgrading processors, and upgrading all

sorts of technology. But we would like to maintain stability in the fundamental architecture for some time.

MIL EMBEDDED: ***To what extent are there requirements on the table or being talked about for coalition interoperability or Non-Governmental Organization (NGO) interoperability?***

BAUMAN: First of all, our MIDS program is a cooperative program paid for by five nations: the U.S., France, Italy, Spain, and Germany. MIDS-LVT was that way, and MIDS-J has financial participation from our allies. Our plan is to deliver a tech data package to them at the end of the MIDS-J core radio development, which is coming up soon. We are also working with those particular countries in terms of them developing their own capability, based on our design (or buying our capability).

We also have the U.K.'s Bowman waveform – through formal qualification tests and in our repository. And as part of our enterprise business model, we are making that waveform available to all vendors so that they can add it to the radios they're already selling. We're hoping that Thales and Harris might port the Bowman waveform to their JEM and Falcon III products that we're already buying, which would allow us to buy that capability from existing contracts. We also have a coalition waveform development effort with primarily European allies, and that's just getting underway. Beyond that, we're also looking at a coalition wideband networking waveform tool to allow networking interoperability among the U.S. and coalition partners.

We have some difficulty with taking our waveforms and giving them to everybody in the world. We have an information repository within the U.S., for U.S. vendors, for U.S. government purposes. For security reasons, it's not quite easy to give that code away to our allies. It's not something that we will probably do directly. But that doesn't preclude us from working on a waveform with our coalition partners, and that's exactly what we're doing.

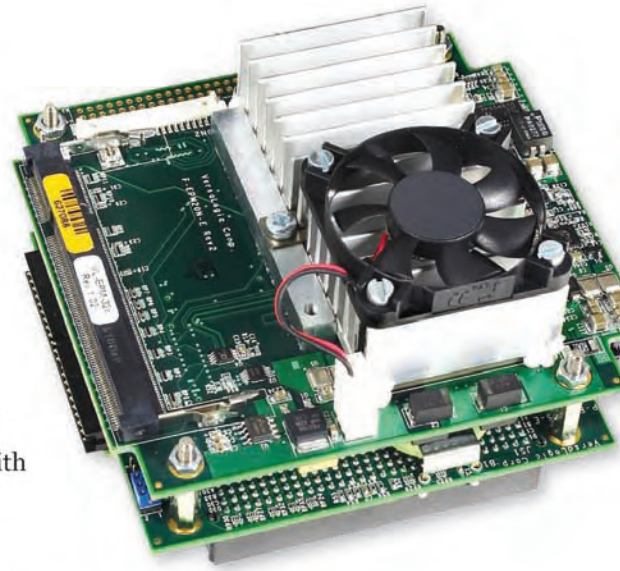
Dennis M. Bauman *has been a Joint Program Executive Officer, Joint Tactical Radio System, since 2005. His current job duties include directing all waveform, radio, and common ancillary equipment development; performance and design specifications; standards for system operation; and JTRS systems engineering. Previous positions include Weapons Officer and Qualified Surface Warfare Officer in the U.S. Navy, Software Manager for the Naval Ocean Systems Center in San Diego, Head of the Operational Systems Branch of the Submarine Communications Division, and SPAWAR Program Director for C2I and Combat Support Applications, among others. He earned his Bachelor's degree from Pennsylvania State University and a Master's degree in Computer Science from the University of California at San Diego. For more information on JTRS, email jpeo_jtrs_help_desk@navy.mil.*

JPEO JTRS
http://jpeojtrs.mil

When You're at 30,000 feet Quality Matters

Our Products and Services are Second to None

At VersaLogic we know about building dependable, high reliability embedded computers for mission critical applications. Our products have been designed into some of the most sophisticated and high profile military and aerospace equipment used today. Every board we make is run through exhaustive inspections and quality tests, ensuring that we deliver only the best. And with our world class service and five year availability guarantee, we'll always be there when you need us. Whether you need one of our standard products or a customized version, our skilled technical staff will work with you to meet your exact requirements. So before your program launches, choose the company with the quality and service to take you where you need to go.



Contact us to find out how for more than 30 years we've been perfecting the fine art of extra-ordinary support and on-time delivery: One customer at a time.

1.800.824.3163
1.541.485.8575
www.VersaLogic.com/jet

VERSALOGIC CORPORATION

Digital-Down Converter implementation, FPGAs offer new possibilities

By Bob Sgandurra and Rich Kuenzler

Photo courtesy of the DoD/U.S. Air Force by Senior Airman Julianne Showalter

Over time, Digital-Down Converters (DDCs) have shifted functionality from ASICs to FPGA IP delivery. The shift brings more optimization suited to many applications, yielding design flexibility and system-level savings. But are FPGAs always better than their ASIC rivals?

Digital-Down Converters (DDCs) have become a cornerstone technology in communication systems. Similar to its analog receiver counterpart, the DDC provides the user with a means to tune and extract a frequency of interest from a broad radio spectrum. Over the past few years, the functions associated with DDCs have seen a shift from being delivered in ASICs to operating as Intellectual Property (IP) in FPGAs.

For many applications this implementation shift brings advantages including: design flexibility, higher precision processing, higher channel density, lower power, and lower cost per channel. During the past three to four years, with the advent of each new higher performance FPGA family, these benefits continue to increase. Bob and Rich, through practical examples, explore some of these key benefits of implementing DDC designs in FPGAs – including more flexible designs and system-level savings on board count, space, and power. But are ASICs ever a better choice than FPGAs?

Digital-Down Converter fundamentals

To understand how FPGAs play a key role in implementing DDCs and performing the function of a receiver, it's important to break the DDC down into its individual functional blocks. Figure 1 shows a classic DDC. Regardless of whether it's implemented in an ASIC or an FPGA, this is a common architecture used to perform the DDC function.

The first stage of the DDC uses a digital mixer to frequency translate a specific channel frequency down to baseband using a pair of multipliers and a Direct Digital Synthesizer (DDS). This function enables the user to tune the receiver to the desired frequency of interest. The second stage of the DDC reduces the sample rate of the signal to match the desired channel output bandwidth using a Cascaded Integrator Comb (CIC) filter to decimate the data. A second CIC filter provides a coarse gain adjustment stage. The signal is then passed to a pair of additional polyphase filters: First, a Compensation Finite Impulse Response (CFIR) filter, then to a Programmable Finite Impulse Response (PFIR) filter. This filter pair provides additional decimation and final signal shaping prior to the rounding stage and final output.

When you get past all the acronyms and realize that most of the individual function blocks of the DDC are implemented using multipliers, it starts to become apparent how the DDC might map into current FPGA families. Most newer FPGAs include a wealth of DSP function blocks that are primarily multipliers.

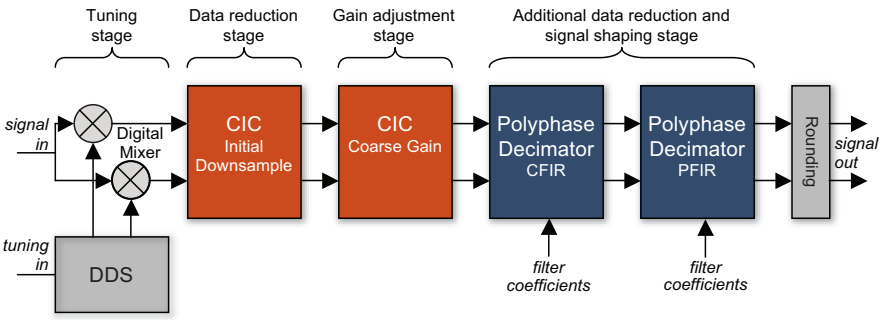


Figure 1

DDC implementation	Number of channels	Decimation range	Input rate (MSps)	SFDR	Tuning resolution	Area per channel (mm²)	Power per channel (W)	Cost per channel (US$)
Xilinx DDC V1.0 core	19	4-1048512	110	108	Integer steps	64.5	.63	78
Pentek 430 DDC core	256	1024-9984	110	110	Steps of 256	4.7	.01	3
Pentek 420 DDC core	2	2-64	110	118	Binary steps	612.5	2.5	420
GC5016	4	1-4096	160	115	Integer steps	72.3	.25	41

Table 1

Additionally, the general-purpose logic resource and on-chip memory of FPGAs also match the requirements of the DDC for implementing the required FIR filters and filter coefficient tables.

Design flexibility: DDCs as intellectual property cores

As part of their intellectual property library series of IP, Xilinx provides a free DDC core. This Digital-Down Converter core is the basic building block of multi-channel DDCs. It follows the classic DDC architecture (Figure 1) and provides a total decimation range of 4 to 1048512. As a generic building clock, it needs to satisfy a wide range of applications and can't really be optimized for a specific range. In addition to the Xilinx core, IP is available from a number of companies providing more options and better optimization to match specific applications. Two of these cores are offered by Pentek, implemented in a Virtex-II Pro 50. The 430 DDC core is optimized for high channel count/narrow bandwidths, while the 420 core is optimized for wider bandwidths and better Spurious Free Dynamic Range (SFDR) but with fewer channels. Table 1 compares these choices with a popular ASIC-based DDC solution from Texas Instruments.

When compared on a size/power/cost per channel basis, it becomes apparent that narrowband, high channel count DDC cores can be very efficiently implemented in FPGAs. Implementation of wideband DDCs tends to consume many more FPGA DSP and logic resources, limiting the number of channels that can fit in a single FPGA, thus reducing the overall savings. But even with less cost-effective wideband DDCs, the custom IP approach can sometimes provide the only viable solution when a specific performance characteristic is required like extended SFDR, for example.

IP enables flexibility in software radio products

Aside from stand-alone IP cores available from Xilinx and other IP vendors, some vendors are offering FPGA-based integrated communications receiver products that offer the IP preinstalled. As stated earlier, custom IP or cores can be optimized to address a specific application, enabling more efficient use of FPGA resources and yielding better performance.

The flexibility this optimized core approach delivers becomes more apparent when products are provided by the same vendor and are actually the same hardware with only changes to the IP core. A system engineer can design a single

hardware receiver product and use it across a range of different application spaces. Additionally, some single applications, like Joint Tactical Radio System (JTRS), need to operate across a wide spectrum to handle diverse signal types. Figure 2 shows three optimized cores versus a non-optimized core across a range of applications, and the number of channels and bandwidths they typically require. Again this wide range of applications can be satisfied by using the same hardware, but different, optimized IP cores. This is one of the fundamental concepts of Software-Defined Radio (SDR), and is difficult or sometimes impossible to achieve with ASIC-based solutions.

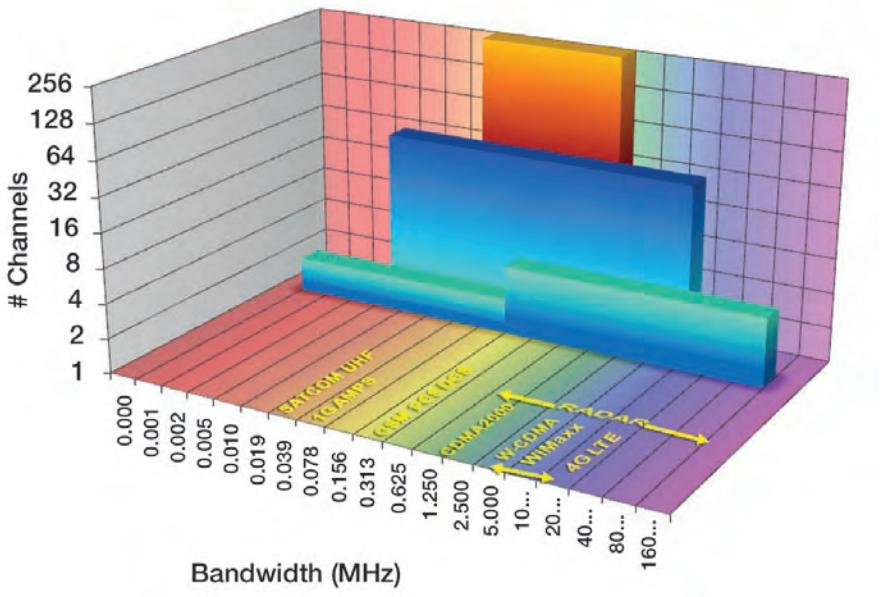


Figure 2

System-level savings

So let's take a look at a complete receiver system. One common application is GSM 2G, a high channel count, low-bandwidth system. An E-GSM receiver requires 174 channels spaced 200 KHz apart. Just three or four years ago, a viable solution would have used TI/Graychip four-channel 4016 ASIC-based DDCs.

A common board form factor for these types of applications is PMC, a compact I/O module for VMEbus systems. One PMC can house two 100 MHz A/Ds and four 4016s and all of the required interface and support circuitry. For a 174-channel system, this would require 11 PMC modules. By comparison, an IP DDC with 174 channels and similar performance to the 4016 can fit in a single Virtex-5 XC5VSX95T FPGA that can be housed on a single PMC, along with two channels of 200 MHz A/Ds and all support circuitry. The PMC board count, along with cost, space, and power, can be greatly reduced as shown in Figure 3.

FPGAs versus ASICs

FPGAs continue to offer new possibilities and performance when addressing processing tasks like Digital-Down Conversion. With each new generation of higher-performance FPGAs, processing precision continues to increase, enabling IP-based DDCs to outperform their ASIC-based cousins with specifications like better Spurious Free Dynamic Range.

From a system-level view, it's easy to understand how packing many channels of DDCs into one or two FPGAs can reduce the board count, power requirements, and cost over a solution that requires 30 or 40 individual ASIC DDC chips to run the same application. Additionally, FPGA solutions can be extremely flexible by supporting vastly different signals with the simple load of an IP core and reusing the same hardware platform.

However, FPGAs are not a perfect match for all requirements. They show the greatest advantages in systems with

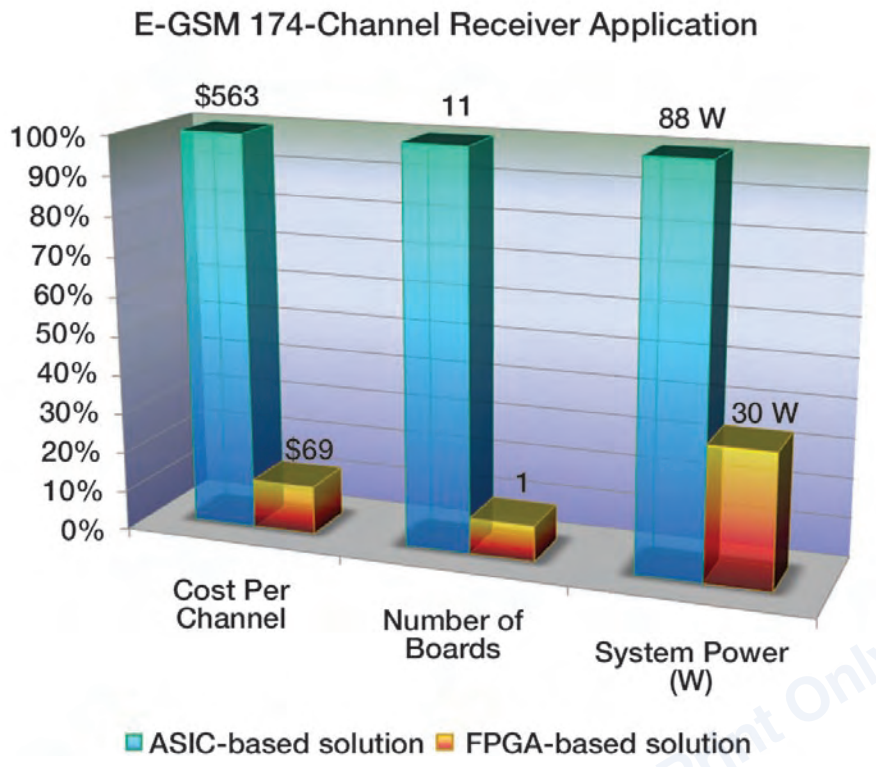


Figure 3

high channel densities and typically narrower bandwidths where many DDC channels can fit on a single FPGA. In systems with just one or two channels and very wide bandwidths in the range of 100 MHz or greater, the higher cost of the FPGAs needed to fit the larger wideband DDC cores can quickly exceed the cost of designing the system with a single multi-channel DDC ASIC.

So, while cost, size, and power are important factors in designing a receiver system, ultimately the technical requirements may dictate the choice of whether an ASIC or FPGA is used.

Richard Kuenzler *is a senior design engineer at Pentek, specializing in the development of DSP, I/O, and software radio hardware products. During his 17 years in the DSP industry, Rich also worked for Hughes and Raytheon where he specialized in image processing and the development of military night vision systems. He holds a Bachelor's degree from Syracuse University and has been published in various electronic industry magazines. He can be contacted at Kuenzler@pentek.com.*

Robert Sgandurra *serves as senior product manager over Pentek's DSP, data acquisition, digital receiver, and software products. He joined Pentek in 1994, working as an application engineer and system integrator, taking on the responsibility of product manager in 1997. Prior to Pentek, he worked seven years in the medical electronics industry designing and managing projects for ultrasound imaging. He holds a BSCS from the New York Institute of Technology. He can be contacted at Bob@pentek.com.*

Pentek, Inc.
201-818-5900
www.pentek.com

FPGAs for mission-critical applications

By Rajiv Jain and Mehul Kochar

Photo courtesy of U.S. Air Force by Senior Master Sgt. Tom McKenzie

Most FPGA technologies fail to address key mission-critical design requirements, but anti-fuse-based architectures succeed, providing essential attributes such as radiation resistance and design security.

Today's high-density FPGAs offer designers an opportunity to quickly create customized components for optimum performance and rapid deployment of mission-critical systems. But for military and aerospace applications, memory-based FPGA technology is known to fall short in addressing several important requirements, including radiation resistance and design security. Anti-fuse FPGA technology successfully addresses these requirements to bring the advantages of programmable logic to mission-critical system design.

Many developers understand that mission-critical systems must be designed for reliable operation in extreme environmental conditions, but find that most FPGA technologies are hard-pressed to meet these needs. Further, there are other requirements that can be just as critical in determining a device's suitability for mission-critical service where most FPGA technologies fall short. Our discussion will focus on three of these other key requirements: nonvolatile configuration, reliable operation in a radiation environment, and design security (Table 1).

Trio of factors affect critical apps

The requirement for nonvolatile configuration arises from the high probability of power interruptions in mission-critical mil-aero applications. Replacing live system components during maintenance or repair, lapses when switching from line to battery power, and brownouts can all trigger a need for the system to recover from power interruptions. A nonvolatile system configuration simplifies the recovery process, eliminating the need to reload system settings and parameters. This makes system recovery quicker and less error-prone than when the configuration must be reloaded, increasing system availability to perform its mission.

Additionally, with the end of the Cold War, the need for mil-aero systems to operate in radiation environments has faded from general awareness. This requirement does not just come from the need to survive nuclear events, however. Even in daily operation, mission-critical systems might be exposed to high

Attribute	Requirement	SRAM FPGA	EEPROM FPGA	Anti-fuse FPGA
Nonvolatile	Quick power-up, quick brownout recovery, design security	No	Yes	Yes
Radiation resistance	High-altitude operation, nuclear battlefield operation, nuclear event resistance	Low	Moderate	High
Design security	Protect data content (passwords, encryption keys, and so on), prevent reverse engineering, prevent design cloning	Low	Low	High

Table 1

radiation levels. The radiation comes in the form of cosmic rays and solar wind along with the high-energy secondary particles these sources generate at high altitudes (see Figure 1[1]).

While the radiation flux is typically not high enough to damage semiconductor devices, it does have an impact on system operation. The radiation's typical effect is a Single Event Upset (SEU): a localized energy spike capable of changing the bit value of a memory cell. Such a change could wreak havoc with system operation if it occurs in a critical location within the FPGA.

Design security is a third requirement of mission-critical system design, particularly military systems. If designs are not secure, enemies can quickly erase any technical advantages that such designs provide by reverse engineering and cloning captured equipment for their own use. Systems might also embed sensitive information such as passwords, encryption keys, and frequency-hopping algorithms. Extracting such information from a captured system would allow an enemy

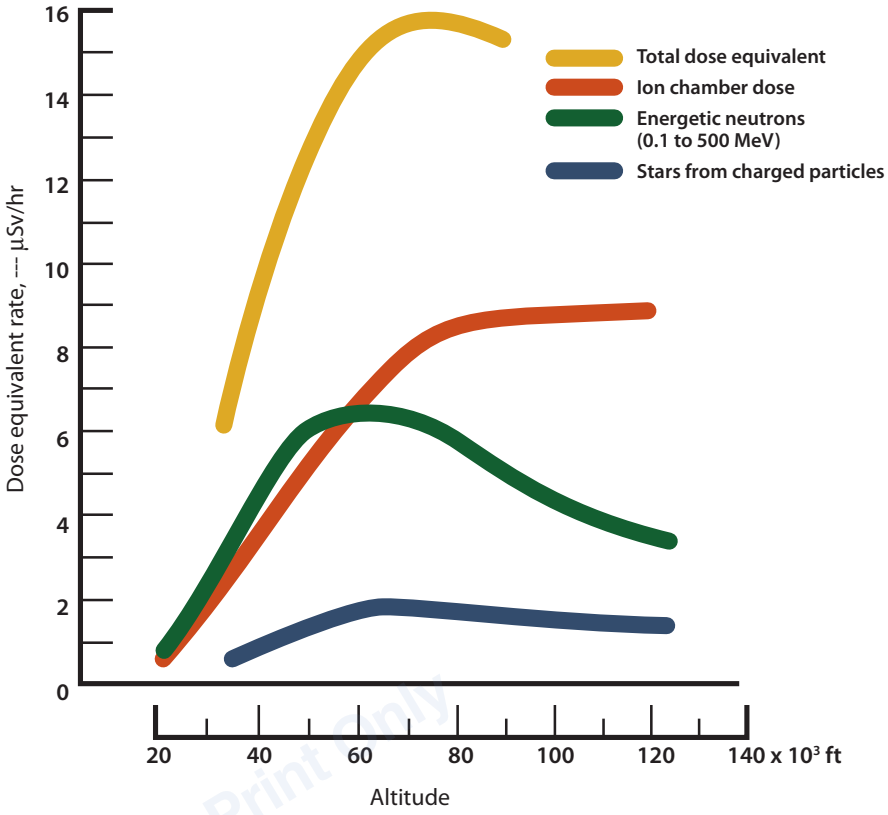


Figure 1

to create equipment that can intercept and interpret coded communications or generate mimicry signals to confound command and control activity. Designs that are difficult, expensive, and time consuming to reverse engineer can prevent such compromises by delaying results until they are no longer useful.

Comparing FPGA technologies

These neglected design requirements are of particular importance when utilizing FPGA technology to develop mission-critical systems. Using FPGA devices gives developers design flexibility and integration levels comparable to using ASICs, but at much lower cost and with more immediate availability. Not every FPGA technology suits the needs of mission-critical design, however.

Many FPGAs fail the nonvolatility requirement, for instance, because they have SRAM as their basis. An internal logic connection in these FPGAs depends on an SRAM cell to hold a switch transistor on or off (Figure 2). The data stored in memory thus determines the FPGA's configuration, but the SRAM cell will lose its data when it loses power.

The SRAM-based FPGA needs to receive configuration data at power-up to prepare it for system operation. The typical approach is to employ a small, external, nonvolatile memory source such as a serial EEPROM to hold the configuration data. Upon power-up, the FPGA retrieves data from the EEPROM and configures itself for operation. Depending on the memory's size and the clock rate at which the FPGA can retrieve data, the FPGA might require several hundred milliseconds following power-up to become ready for use. The rest of the system must wait until the FPGA is ready in order to become fully operational.

The SRAM approach to programmable logic also has several unfortunate design attributes. One is that the circuit needed at each connection point is fairly large, requiring multiple transistors to form the SRAM cell and resulting in lowered interconnect density. The interconnect capacitance of the switch transistor adds to the FPGA's dynamic power dissipation, increasing junction temperatures and lowering device reliability, and the leakage current of the large memory cell wastes power even when not clocking.

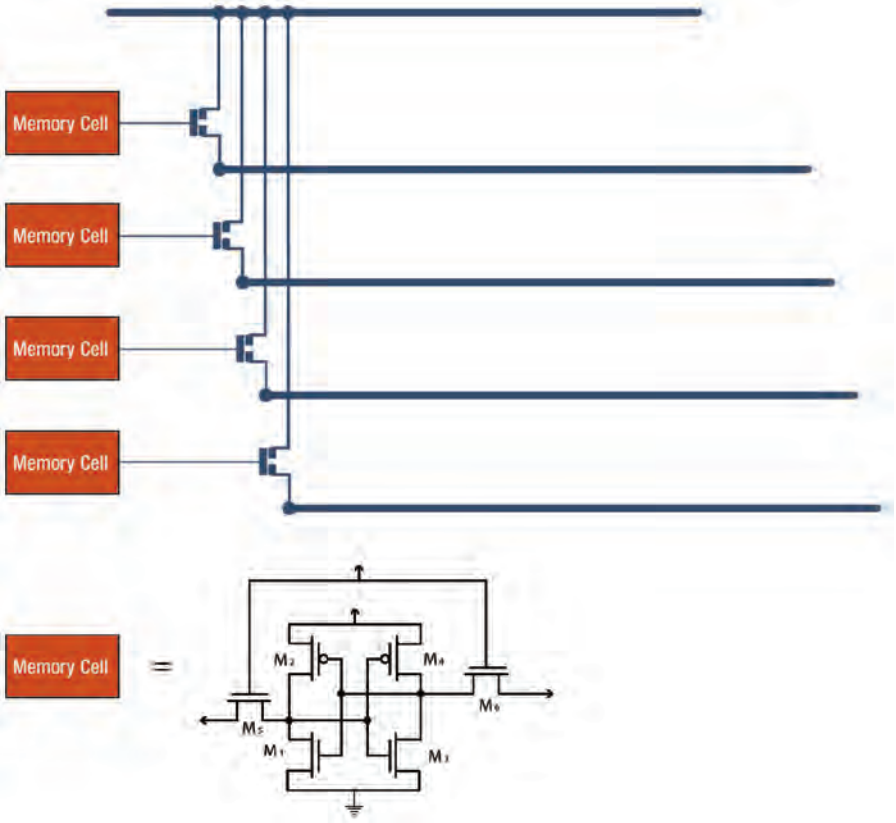


Figure 2

SUPER ★ TALENT®
THE BEST MEMORY

Reinventing Storage

Rugged, Reliable, Unparalleled

SATA / IDE SSD

Solid State Drives

SATA/ IDE SSD

- SATA I, SATA II, IDE and ZIF Interfaces
- 100% compatible with standard hard disk drives
- Form Factors in 1.3"/1.8"/2.5"/3.5"

Now up to 120MB/Sec!

• Performance

Operating Temp: Industrial and Commercial Temperature available
Access Time: 0.1ms
Power Consumption: 85% less than Average HDD

• Reliability

Shock: 1500G(operating)
Vibration: 16G(operating)
MTBF: >1,000,000

• Endurance

Read: unlimited

DuraDrive - Ultra Rugged and Reliable SSDs
MasterDrive - Ultra Fast Commercial SSDs

"AWARD WINNING PRODUCT"

CeBIT
"Innovation of the year" Award

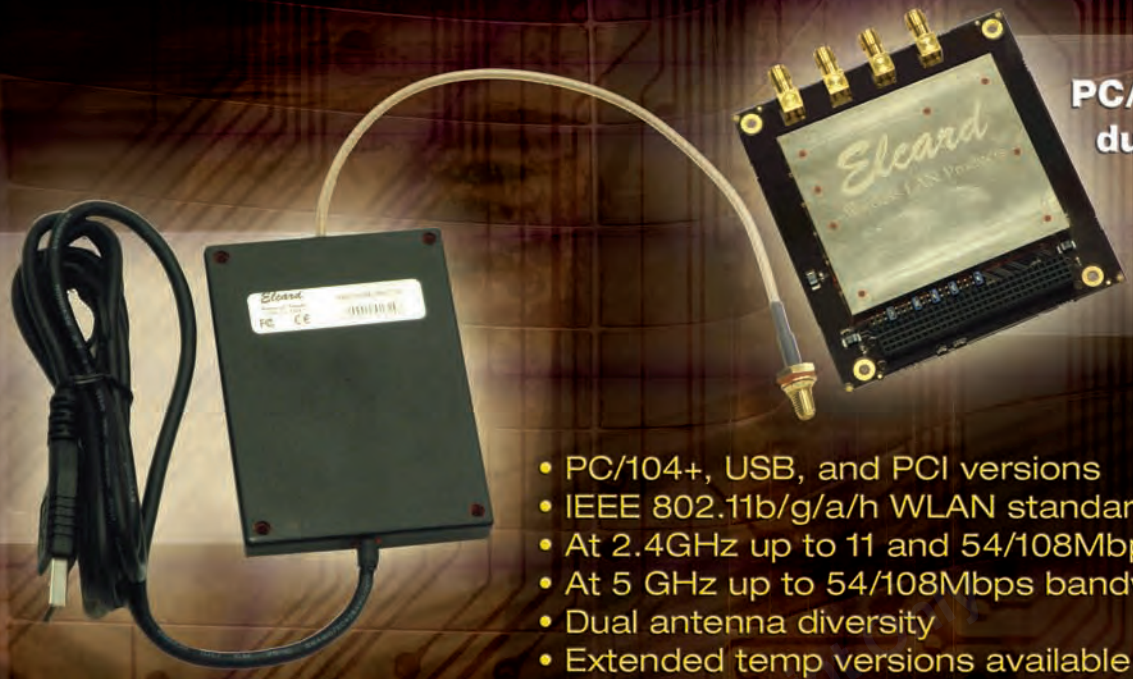
DISKCON USA
Best of Show Award

For more information, please contact :
oemsales@supertalent.com or 1.408.934.2578

ssd.supertalent.com

Elcard™ Wireless LAN Modules

Designed for Industrial and Professional Applications



PC/104+ WIB4xx dual WLAN module

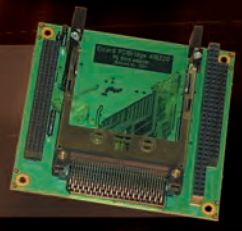
USB-attached WLAN

- PC/104+, USB, and PCI versions
- IEEE 802.11b/g/a/h WLAN standards
- At 2.4GHz up to 11 and 54/108Mbps bandwidths
- At 5 GHz up to 54/108Mbps bandwidths
- Dual antenna diversity
- Extended temp versions available (-40°C to 85°C and -20°C to 70°C operating)
- Rugged and shock resistant, high altitude operation
- Long term supply
- O/S support for Linux, Microsoft™ Windows™ XP/2000/NT/98SE/ME

Rugged Access Points Available

- Dual WLAN versions available (WIB400 series)
- Evaluation kits for easy start-up
- Ranges of 1 mile+ can be reached even at 100mW Tx power with our directional antennas
- Ranges of several miles can be reached with our power amps and special antennas
- WIB250 WLAN module provides dual band 802.11g/ 2.4GHz & 802.11a/5GHz with two antenna connectors

-40°C to +85°C Operating Temperature Range Versions Available



AIB220 PC/104+ Cardbus

- Cardbus/PCMCIA Adapter
- Dual Type I/II or single Type III
- Linux and Win9x/2K/XP support
- 3.3V and 5V card support
- TI PCI1420 chipset

Elcard

Elcard USA
10849 Kinghurst, Suite 105
Houston, Texas 77099
Toll Free: 800-688-4405
Phone: 281-568-4744
Fax: 281-568-4604
Email: sales@elcard-usa.com
Web: www.elcard-usa.com

> “In SRAM, an SEU can invert the state of an individual bit, which the memory circuit will then maintain. In an EEPROM, the SEU can discharge the floating gate, causing a permanent bit change.”

One nonvolatile approach to programmable logic has a similar switch structure but uses an EEPROM cell rather than SRAM to hold the configuration. This approach solves the volatility problem but still shares many other attributes with SRAM-based FPGAs. The architecture still requires a switch transistor at each connection point, limiting interconnect density and signal speed through the connection.

The EEPROM cell works by holding a charge on a floating gate to keep the switch transistor turned on or off. The floating gate receives or loses its charge when a high-voltage programming signal drives electrons onto or off of the gate by tunneling through an oxide layer. In normal operation, the gate has no discharge path available, thus making the FPGA configuration nonvolatile.

An alternative approach to providing nonvolatility is to use anti-fuse technology. The anti-fuse is an amorphous silicon via at each configurable circuit junction in the FPGA. Unprogrammed, the via is an insulator and there is no connection at that site. Programming the via by applying a high voltage to it changes its state to become a conductor, thus making a connection at that site. The physical state of the vias therefore holds the FPGA's configuration. The state change is permanent, making the anti-fuse FPGA nonvolatile. Because no transistors are involved in maintaining the logic connection, interconnect density is high and there is no leakage current. Interconnect capacitance is low, reducing dynamic power.

Addressing radiation

Aside from the issue of volatility, the need to operate in a radiation environment is a second strike against memory-based FPGA technologies. Highly energetic particles passing through an active semiconductor device create temporary ionization paths through the silicon. These pathways can briefly short circuit transistors, creating the transient pulses called *SEUs*.

In SRAM, an SEU can invert the state of an individual bit, which the memory circuit will then maintain. In an EEPROM, the SEU can discharge the floating gate, causing a permanent bit change. While memory used in processor

applications often includes error correction and detection to handle such events, the configuration memory of FPGAs has no such protection. An SEU can thus introduce a persistent logic change in a memory-based FPGA.

The anti-fuse FPGA has no such vulnerability. The energy of an SEU is not high enough to program a via, and the transient pulses have no significant effect on the logic. Tests conducted at NASA/Goddard have shown no errors in anti-fuse FPGA operation at radiation energies as high as 193 MeV, while memory devices begin exhibiting bit errors as low as 100 MeV.

Anti-fuse FPGAs also address design security more effectively than memory-based FPGAs. To completely characterize a programmed FPGA, two pieces of information are required: the configuration details and the underlying structure. Configuration details are the easiest to capture in memory-based FPGAs. With live systems, passive probing can capture programming data as it moves into an SRAM-based FPGA during configuration. Electron probing can determine the charge states of EEPROM configuration cells when the circuit is active. Both approaches are relatively quick to perform and inexpensive to implement.

Determining the logic structure of the FPGA requires more effort, but reverse engineering approaches are available that can extract a device's design details for under $100,000. The approach is to strip away each layer of a logic device, one at a time, using plasma (for passivation and oxide layers) or chemical (for metal layers) etching, then take a high-resolution photograph as each layer is revealed (Figure 3). The photographs allow reconstruction of the mask sets used to fabricate the device. This then permits the device to be analyzed or even cloned.

Investigating the programming of an anti-fuse FPGA, however, requires much more elaborate measures. This results in part because the programmable element lies within a multi-layer structure, so surface scanning is ineffective. Also, there are no signals or stored charges to probe; program storage is a structural change that affects resistance, not an accumulation of charge.

Only physical examination will show the programming state of the anti-fuses, and the layer-stripping method will not work effectively. The cross-section of the altered region in the anti-fuse is too small to observe from above, so the only way to reliably see the structure is from the side (see again Figure 3). Obtaining this view requires the use of a Focused Ion Beam (FIB) to create a trench in the device, then milling the edge to expand the trench in steps. Taking photographs at each step allows creation of a 3-D image of the circuit. This procedure requires expensive equipment, however, and is prohibitively time consuming without foreknowledge of where to look. Even with foreknowledge, the number of anti-fuses requiring examination makes the task impractical. The time required to reverse engineer programmed anti-fuse FPGAs – such as QuickLogic's QL1P075 and QL1P100 – makes them, in effect, absolutely secure.

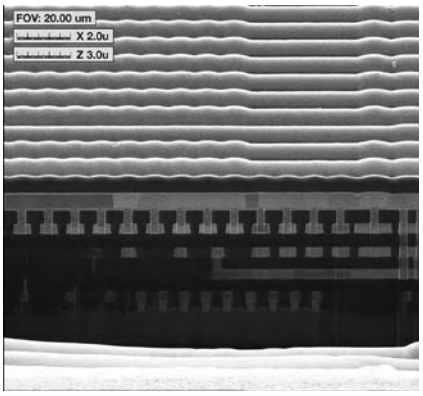


Figure 3a

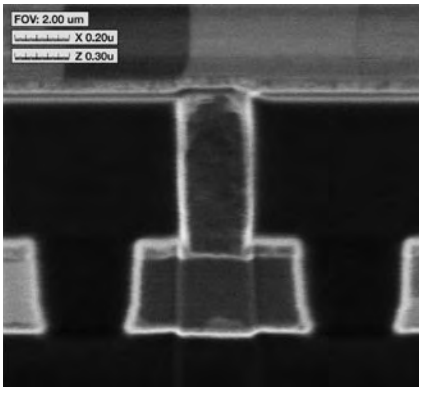


Figure 3b

Anti-fuse satisfies mission-critical needs

The design security needs of mil-aero applications, along with radiation resistance and nonvolatility, are often neglected in literature, but cannot be ignored by designers. When seeking the benefits of FPGAs in design, developers habitually look for devices that address mil temp operation, but they should also consider the base technology's ability to address the aforementioned needs. Of the FPGA technologies, anti-fuse programmability is the only one that meets all the requirements of mission-critical designs.

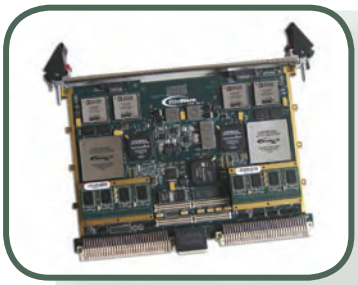
Rajiv Jain *is director of process technology at QuickLogic Corporation, where he has been employed since 1992. He holds a Master of Science degree in Chemical Engineering from the University of California, Berkeley and a Bachelor of Science degree in Chemical Engineering from the University of Illinois, Urbana. He can be contacted at Jain@quicklogic.com.*

Mehul Kochar, *marketing manager FPGA solutions, has been working at QuickLogic for five years, three of which have been in his current position. Previously he attended the University of Tennessee Space Institute for his Masters degree. He can be contacted at Kochar@quicklogic.com.*

QuickLogic
408-990-4000
www.quicklogic.com

References:

1. NASA presentation, "Atmospheric Ionizing Radiation (AIR): Analysis, Results, and Lessons Learned From the June 1997 ER-2 Campaign," Edited by J. W. Wilson, I. W. Jones, and D. L. Maiden, Langley Research Center, Hampton, Virginia; and P. Goldhagen, DOE Environmental Measurements Laboratory, New York, New York, Feb. 2003.



VXS, conduction-cooled VME combine FPGAs and TigerSHARC DSPs

BittWare was once known as an exclusive Analog Devices SHARC supplier. In fact, the company was a leading supplier of SHARC boards and routinely "beat up" on PowerPC designs[1]. No more. Over the past 18 months, the company developed their so-called *hybrid architecture* to combine the best of both worlds: SHARC or CPU plus Altera FPGA. Their latest product is one we overlooked earlier this year, though it did appear in the May issue of this magazine under New Products: the GT-6U-VME (GTV6) VITA 41 VXS board. Combining twin Stratix II GX FPGAs, two ADSP-TS201S TigerSHARCs, and 3 GB of DDR2 SDRAM, the conduction-cooled board is designed to marry reconfigurability with the SHARC's legendary flow-through DSP architecture.

Targeting radar, sonar, unmanned vehicles, and SDR, flexibility with speed are the core tenets of this board. It supports 5 GBps of simultaneous external I/O and 14.4 GFLOPS of floating point math capability. As well, it's fully programmable – owing to the SHARC's flexibility and the infinite reconfigurability of those FPGAs. BittWare's ATLANTiS software framework marries the components nicely, handling I/O routing and interprocessor/FPGA communication and loading. A custom bridge chip supports 32-bit, 66 MHz PCI and GbE. Tundra's Tsi148 then bolts PCI to VME.

[1]The other leading SHARC provider was Transtech DSP, which was acquired by VMETRO … which is now an acquisition target by Curtiss-Wright Controls Embedded Computing. Food for thought on SHARC suppliers.

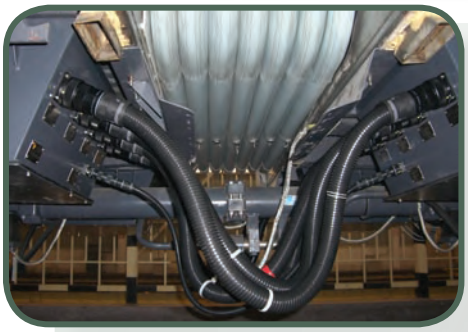
BittWare • www.bittware.com • RSC# 36356

Toughbooks now include Core 2 Duo

First, the good news: Panasonic's semi-rugged CF-52 and CF-74 notebook computers are now available with Core 2 Duo processors and labeled with *Intel Centrino 2* technology. Second, the bad news: It's hard to figure out exactly what "Centrino 2" means. Intel's confusing nomenclature notwithstanding, the 15.4" CF-52 and sunlight-readable 13.3" CF-74 notebooks are now up to speed with Intel's – ahem! – almost newest notebook processors (just wait a few months). We say that like it's a bad thing. On the contrary: Panasonic's Toughbook series is the gold standard for fully- and semi-rugged military laptops.

The company reports that more than 500 checks and tests go into every product before shipment, and that the CPU change is the first major upgrade in each product in more than 12 months of stability; this is a good thing, in light of consumer products like notebooks going obsolete in as little as three months. At the recent Intel Developer Forum, we got a chance to drop-kick a Toughbook and witness a spill test on the keyboard. These babies are tough, and keeping them production stable in their nice magnesium alloy cases with their shock-isolated HDDs is essential for mil duty. Besides the processor upgrade – which when added to the CPU chipset and WiFi radio comprise "Centrino 2" – hard drive capacity goes up to 160 GB, and WiFi gets pumped up to 802.11 Draft N.

Panasonic Computer Solutions Company • www.panasonic.com/toughbook • RSC# 38570



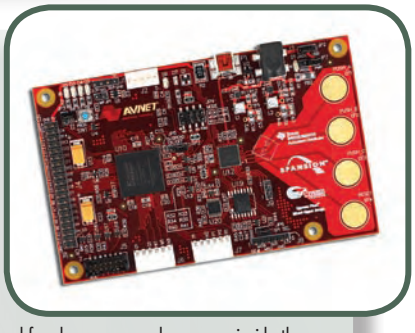
COTS vehicle junction box

Developed originally for mass transit applications, the ITT Interconnect Solutions VEAM junction box assembly contains a complete harnessing system for in- and inter-vehicle electrical connections. We can picture the units installed in light rail applications (shown), but the box is just as applicable in light-duty military applications that don't call for 38999-style screw-on cable assemblies. With rapid deployment the norm these days, add-in COTS equipment latched down to HWMMVs and TOCs still needs to be rugged, but not necessarily to the extent of requiring high-cost MIL-SPEC cable assemblies.

The VEAM includes terminal blocks, cables, and other electrical components designed to provide signal and power. Though each implementation is a custom solution, the target types of functions include control switchboards, CCTV equipment, inter-vehicle comms, power and signal, and motor supplies up to a whopping 660 A. The junction boxes are approved to IP66 standards (Ingress Protection, wet conditions), contacts are rated to 400 A, and the shells and contacts come in a wide variety of configurations. VEAM boxes are available in either standard or harsh environment versions, and complete systems can be tested to meet specific electrical, shock, and vibration specs.

ITT Interconnect Solutions • www.ittcannon.com • RSC# 38571

Here's a twist: Add SoC to offload FPGA



Face it, programming FPGAs is difficult. So when Avnet introduced their Xilinx Spartan-3A FPGA Evaluation Kit earlier this year, designers rushed to plunk down $39 and snap up a couple thousand of them. And why not? Here was a stand-alone platform to tinker with to their heart's content. Turns out that adding an external programmable microcontroller to the FPGA can save design time, FPGA gates, and power. So Avnet and Cypress teamed up, bolted on the Cypress CY3217 Programmable SoC, and magically added up to 100 peripheral functions *outside the FPGA.*

The PSoC enables FPGA configuration and flash memory programming through a built-in USB interface instead of the typical cumbersome serial PROM. Cypress' MiniProg programmer and downloadable PSoC Designer software add not only the USB feature, but also CapSense touch sensing, clocks, and programmable analog functionality (you know: all those real-world HMI thingys without which a defense system is nothing more than a current sink). In short, this simple external device has greatly enhanced the FPGA eval kit, simplified tabletop designs, and freed up power and resources inside the Xilinx FPGA. Seems like a good trade-off to us.

Avnet Electronics Marketing, Americas • www.em.avnet.com/spartan3a-evl • RSC# 38572

Continued on page 45


Keep Your Design...
Change Your Perspective.
It takes creative thinking to launch breakthrough solutions. Whether we optimize board space, work with environmental extremes or solve component incompatibilities, be assured that your design can be realized with our advanced microelectronics solutions. See your great ideas take flight at www.whiteedc.com/design.
602.437.1520 TEL | 602.437.9120 FAX
WHITE ELECTRONIC DESIGNS
www.whiteedc.com
Customer First. Quality Always.

We Simplify Technology

CORE SYSTEMS

Reliable operation in severe environments

- Integrates hardware mechanically, electrically and thermally
- Fanless, total thermal solution
- Mini PCI & PC/104 expansion
- MIL–810F, EN50155 available
- Installed Windows® XPe or Linux available
- Virtually indestructible mobile power supply
- NEMA 4X
- –40° to 85° C

- Transportation
- Mining vehicles
- Outdoor kiosks
- Industrial servers

- Digital signage
- Military and police
- Traffic management
- Digital video surveillance
- Asset management

303–430–1500

OCTAGON SYSTEMS

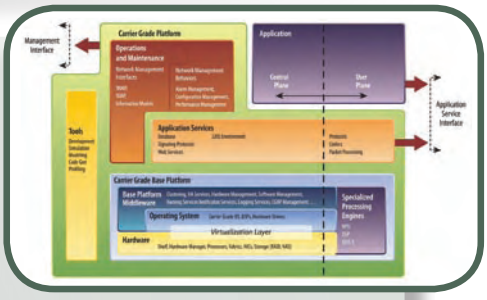
www.octagonsystems.com

Nonvolatile RAM for mission-critical systems

SRAMs are fast, but take away Vcc and *poof!* There goes your data. On the other hand, flash memories retain data when they're off, but they're woefully slow when used in place of scratchpad RAM. One compromise between the two is Freescale's Magnetoresistive RAM (MRAM), now available in two extended temperature ranges from e2v Technologies. e2v is a longtime partner, going all the way back to providing military versions of then-Motorola's PowerPC product line.

MRAMs combine nonvolatility with SRAM speed plus the density of DRAM. Unlike flash (which uses trapped charges in the silicon bulk) or SRAM (which stores bits with conducting transistors), MRAM works by creating magnetic switches on a nanoscopic grid and storing data as electric fields. e2v's EV2A16A 4 Mb MRAM operates at SRAM speeds of 35 ns read/write, while still offering a standard SRAM interface to make system design a breeze. The 44-lead TSOP device is available in extended (-40 °C to +110 °C) and military (-55 °C to +125 °C) temperature ranges.

e2v Technologies • www.e2v.com • RSC# 38565



Carrier-class software package for AdvancedTCA

While the telcos continue to adopt PICMG's AdvancedTCA form factor at their own pace, the military is deploying AdvancedTCA (and its mezzanine board, Advanced Mezzanine Card or AMC) for high-density deployed networks and phone systems. This essentially is creating POTS-like VoIP with all the features of a local Internet cloud, including voice, video, and high-speed file movement. Enea has developed its Accelerator Platform 2.0, the second generation of a software package designed specifically to provide carrier-grade telco services for Kontron AdvancedTCA boards and platforms providing IP-based broadband, VoIP, IPTV, gaming (as in *America's Army)*, and streaming video.

Enea claims this is the first application-ready platform to "integrate a carrier-class Linux OS with middleware, network protocols, embedded management, database software, and DSP management." The 2.0 version adds support for fine-grain, in-service software upgrades – a critically important attribute in deployed military WANs. Mixed application version management takes the guesswork out of incremental upgrades. Other new features include SA Forum Availability Management, DSP management for data plane blades equipped with DSP farms (think: YouTube codecs or on-the-fly audio processing), HPI shelf management, and support for ConfD. The package also works with Embedded Planet's and Mercury Computer's AdvancedTCA/AMC-based DSP and PowerPC hardware.

Enea • www.enea.com • RSC# 38566

Intel inside ... everything on the battlefield

(and above it, and below it.)

By Chris A. Ciufo, Editor

I'm a semiconductor guy by training and a gadget geek by choice. These traits cross paths at only one conference each year: the Intel Developer Forum[1]. This past August, the four-day U.S. show consumed all three floors of Moscone West in San Francisco, hosting almost 3,000 attendees, including nearly 800 journalists/analysts (me included[2]). Intel took the wraps off several processor roadmaps including Nehalem and future Atom CPUs (Menlow XL), announced groundbreaking partnership programs with the likes of DreamWorks and Yahoo, described its vision of the fourth wave of the Internet and mobile Internet devices, launched its first pure consumer multimedia SoC for televisions, and even re-entered the storage market with a line of superfast solid-state disks. The list of announcements was so far-reaching that *I guarantee much of this will find its way into the military market* within the next several years. Following are some of those I consider most relevant to defense[3].

The fourth wave of the Internet

The Internet has evolved technology from 1) mainframes, 2) servers and PCs, 3) cell phones, and now to 4) always-connected embedded devices: the so-called *fourth wave of the Internet.* Intel's R&D is driven by predictions for an estimated 15 billion connected devices by 2015, with anchor technologies in Intel Architecture (IA) processors, low-power Atom CPUs and SoCs, encryption and storage, IPv6 by 2012, and connectivity including WiFi, WiMAX, Bluetooth, and ZigBee. Intel coined the term *Mobile Internet Devices* (MIDs), which can be considered handheld battery-operated devices, infotainment platforms such as IP home telephones, automotive telematics systems for navigation or entertainment, and even telemedicine equipment used by rural physicians in third-world countries (from where the company says the majority of device growth will come).

Demos of all these live video and mnemonics-equipped platforms occurred onstage; it doesn't take too much imagination to extrapolate the BMW demo into a dismounted soldier's situational awareness display featuring "birds eye" battlefield data.

As for concrete devices, Intel's sub-1 W Atom CPU was introduced in the spring, has secured "over 700 design engagements," and will clearly be the cornerstone of the company's embedded efforts. The Atom "Low Power IA" and the EP80579 integrated SoC are planned for 2008 (the company's first IA SoC since the 80386EX in 1994). These will be offered in industrial temperature, on the *embedded roadmap* for extended life cycle, and boast a 45 percent area savings and 30 percent power reduction. Each will spawn unnamed new devices in 2009, code named *Menlow XL* and *San Onofre,* respectively. Intel also promised to shrink the already low-power Atom (0.65 W currently shipping) down to ARMcore territory – which means milliwatts in standby mode for cell phones and other low-power doodads.

The company also revved up the previously announced Moblin initiative (www.moblin.org). This Atom-based, Linux-equipped organization provides hardware and software pieces for MIDs. Nearly 20 companies demoed products and application software, but one of my favorites was GyPSii – a location-based "Social Networking App" that mashes up friends' locations with maps and points of interest. If run on a secure network, this could *easily* be a COTS-based Blue Force Tracker. Another application from OneVoice Technologies provides a user-independent voice recognition interface for MIDs – also useful for C4ISR handhelds operated by Marines wearing gloves who can't punch dinky keys.

Nehalem: Core i7

For the past several years, Intel has been developing products based upon their *Tick-Tock Development Model*: first a new microarchitecture such as 65 nm Merom ("tock"), followed 45 nm Penryn process shrink ("tick"). Merom and Penryn are the basis for Intel Core (and Core 2, Core 2 Quad, and so on) CPUs. With the next "tock" on tap, Intel's Nehalem finally adds an on-chip memory controller; will be available in two, four, or eight cores; and extends HyperThreading up to eight 2-way simultaneous multi-threads and the new SSE 4.2 instruction set.

Nehalem is Intel-significant because their entire CPU product line branches to either Nehalem or Atom derivatives. When coupled with the X58 chipset, the first Core i7 devices add *Turbo Mode*, *Power Gates, 8-way Threading*, and boast nearly a 2x increase in 3-D graphics and a 3x increase in memory bandwidth. This is also the first Intel architecture to use the faster, more expensive three-channel DDR3 memories. The first (Nehalem-EP) will be available late in 2008 as a server chip in the Core i7 family. Desktop and mobile versions (Havendale, Lynnfield, Auburndale, and Clarksfield) follow in late 2009. Suffice it to say, I've not even scratched the surface of just Intel's announcements at IDF.

[1] If the bonanza that is the Consumer Electronics Show (CES) were more tech than show, it would probably top my list. But IDF is a layer cake of hard-core tech, iced with cool new gadgets and future visions.
[2] I snapped more than 1,000 photos of slideware, giving me a comprehensive record of IDF information.
[3] Full disclosure: *Military Embedded Systems* magazine was one of the media sponsors of the event.

GE Fanuc
Intelligent Platforms

There's laboratory testing. And there's battle testing.

What we've learned in the field goes into every rugged board we build.

Over the decades, our single board computers and rugged systems have seen significant action. During deployment, they have often taken a great deal of abuse. And this experience has given us real world expertise that cannot be gained in the laboratory.

These lessons of battle inform our entire rugged product design process, of which the new VG6 single board computer is the latest example. The VG6 takes rugged 6U VME multiprocessors to an entirely new level with Dual or Single Node 8641D processors from Freescale®, up to 3 GbE ports, 2 fast Ethernets, 6 USB, 2 SATA and 2 PCI-X capable PMC slots. However, it is also firmly based on a proven design, the VG5, and on a proven PowerPC® processor family. Decades of experience have demonstrated the wisdom of building on a successful design, adding new capabilities, and doing all we can to prepare for the rigors of deployment.

In the field of rugged computing, there is simply no substitute for experience. Fortunately, our systems have been deployed for many years by the land, sea and air forces of the world, and we have learned from that experience. The result is a product offering that encompasses scores of rugged boards and systems in VME, VPX, cPCI. For more details, visit **www.gefanucdefense.com.**

VG6
Conduction Cooled
-40 to +85 C, 40g shock

GE FANUC

GREAT PERFORMANCE CAN COME IN SMALL PACKAGES

More in less. It's become the mantra for space, weight and power constrained embedded systems. The good news is that the 3U VPX bus architecture is a game changer, combining previously unreachable bandwidth in a highly rugged small form-factor.

Now, you truly can have more performance in a smaller package. Curtiss-Wright's 3U VPX VPX3-127 single board computer is the proof. It combines a single/dual-core high-speed Freescale 8640D Power Architecture processor with extensive I/O. Its VPX backplane and 64-bit PMC/XMC connectivity deliver jaw-dropping multi-GB/sec data rates. And a rich set of I/O maximizes flexibility with PCIe or SRIO fabric ports, two gigabit Ethernet ports, 4 serial channels, up to 8 bits of discrete digital I/O, and USB 2.0 ports. Even better, there's no compromising on memory, with options for up to 2 GB DDR2, 256 MB NOR FLASH and 1 GB NAND.

With unmatched performance and versatility in a small form-factor package, Curtiss-Wright's 3U VPX3-127 SBC delivers a highly capable processing platform for a wide range of embedded military and aerospace platforms from tactical aircraft and armored vehicles to naval systems. Now, small really is beautiful.

And it's rugged, too.

VPX3-127

The VPX3-127 Single Board Computer is Curtiss-Wright's newest next-generation 3U VPX SBC for your space, weight, and power constrained applications where performance is key.

CURTISS WRIGHT Controls
Embedded Computing

Innovation In Motion.
cwcembedded.com

3U VPX SBCS... ABOVE & BEYOND

MIL/COTS DIGEST

The Defense Electronic Product Source

September 2008

In This Issue

Atom, Ethernet, and Intelligence

Three vowels affecting the military vernacular in small form factors

MIL/COTS DIGEST will become a regular supplement to *Military Embedded Systems* magazine in 2009. The response to our "VME Products" special in July was quite favorable, so this month we have another themed supplement: Small Form Factors (SFFs).

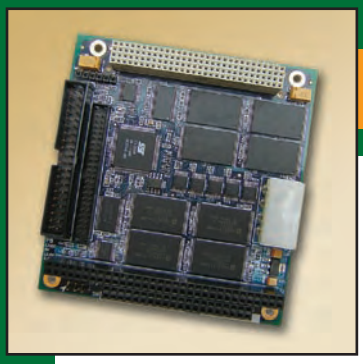
Despite the appeal of 6U VME and CompactPCI in exceptionally rugged systems, the trend toward SFFs in deployed military platforms is unmistakable. And why not? Their smaller size allows them to be tucked into avionics bays, cocooned in smaller bespoke chassis, and even soldier-mounted or hand-carried into battle. Smaller also means lighter weight, which itself means lower mass and increased shock and vibration tolerance. They're usually lower-power systems too, since their size constrains the amount of heat they can dissipate.

My editors and I have selected products that best epitomize semi- or really-rugged SFFs. We noticed some interesting trends among the products that made the cut. First, Intel's ***Atom*** processor is taking the SFF market by storm, finding homes in board standards by PICMG, the PC/104 Consortium, and the SFF-SIG.

Next, ***Ethernet*** continues to be deployed in the military. PMC and XMC modules now offer TCP/IP or UDP/IP accelerators[1], and SFF carrier-grade products from Omnitron sport DWDM and CWDM long-haul defense WANs. Finally, ***Intelligence*** can be found in abundance in these SFFs. From FPGAs to high-end CPUs, this crop of products is smart enough to do battle with the biggest boards on the planet.

Chris A. Ciufo, Editor

[1]As we went to press, Mercury Computer selected AdvancedIO's V1021 (shown herein) for the company's SR-110 VME VXS-based gateway product.



Solid-state storage module

FlashDrive/104 is a solid-state storage module, providing storage for rugged applications. It uses the latest NAND technology and fits any PC/104 or PC/104-*Plus* stack. It also accesses flash using industry-standard ATA or IDE interfaces. Engineered with harsh conditions in mind, this solid-state drive has no moving parts and delivers high performance and reliability in any environment. High-density flash memory offers large storage capacities and consequently reduces latency for rapid data transfer. The module provides a read/write rate up to 10 MBps, and 4, 8, 16, or 32 GB models are available. FlashDrive/104 features a standard operating temperature range of 0 °C to +70 °C and an industrial temperature range of -40 °C to +85 °C.

www.connecttech.com **CONNECT TECH INC.**

SFF mission computer

DuraCOR 820 is a small form factor tactical mission computer. Powered by the low-power 1.4 GHz Intel Pentium M architecture, it features a lightweight metal chassis weighing less than 3 pounds and measuring approximately 7" x 4" x 3". Because it's preloaded with a Linux image or Windows XPe evaluation license, it boots up out of the box. DuraCOR 820 also includes ultra-miniature MIL-D38999-like connectors. Designed to meet MIL-STD-810F, MIL-STD-461E, and MIL-STD-704E, the computer is suitable for applications such as (un)manned vehicle mission processors, command and control on the move, and rugged computing applications.

www.parvus.com **PARVUS**

High-performance PC/104 SBC

The Athena II SBC is a high-performance, compact PC/104 form factor SBC combining state-of-the-art CPU technology with high-accuracy data acquisition circuitry, all on a single compact board with PC/104 expansion capability. The SBC comes equipped with the VIA Mark CPU, operating fanless at both 500 MHz and 800 MHz speeds over the extended operating temperature range of -40 °C to +85 °C. It also provides 256 MB of soldered-on memory, compared to the 128 MB on Athena. The data acquisition models now include auto-calibration for improved accuracy and a larger A/D FIFO for reliable, fast sampling rates.

www.diamondsystems.com **DIAMOND SYSTEMS CORPORATION**

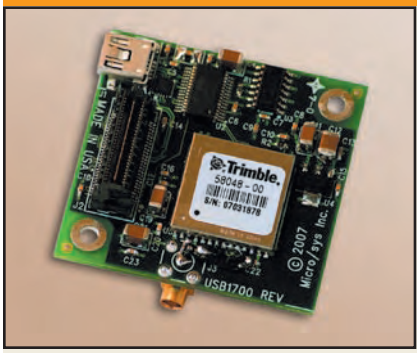
Credit card size FPGA, storage

The Titan-V5e is a credit card size COTS processing module measuring 2.125" (W) x 3.375" (L) x 0.25" (H). It supports Xilinx Virtex-5 FX70T and Virtex-5 SX50T FPGAs, with options for Virtex-5 FX30T, Virtex-5 SX35T, Virtex-5 LX30T, or Virtex-5 LX50T. Titan-V5e utilizes Linux 2.6 with real-time modifications. Three banks of DDR2 SDRAM up to 533 MHZ are provided, at 128 MB per bank. Other features include two Ethernet interfaces using the Virtex-5 TEMAC and removable Secure Digital (microSD) flash up to 32 GB. In addition, the module stores OS, FPGA configuration, and user data.

www.iveia.com

IVEIA

StackableUSB GPS receiver



The USB1700 is a small StackableUSB GPS receiver board for high performance in foliage-canopy, multipath, and urban-canyon environments. At 1.85" x 1.78", the USB1700 is 1/4 the size of the 104 footprint. The board is RoHS compliant and offers 12-channel, WAAS-capable GPS functionality for space-sensitive applications. It also provides extremely fast startup times and operates at a temperature range of -40 °C to +85 °C.

www.embeddedsys.com

MICRO/SYS, INC.

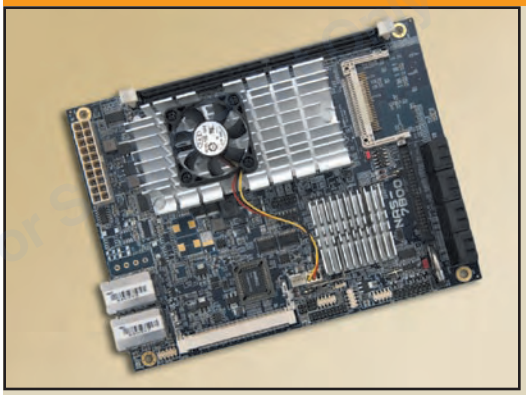
Credit card size module

Kontron's nanoETXexpress-SP is a credit card size COM Express compatible module based on the Intel Atom processor Z5XX series at 1.6 GHz and Intel SCH US15W. The nano-sized module (55 mm x 84 mm) is based on COM Express Pin-out Type 1. I/O comprises Serial ATA, PCI Express, Ethernet, and USB 2.0. Up to 1 GB onboard memory and up to 4 GB flash drive are provided. Other highlights include reduced thermal design power and an integrated memory and graphics controller. The nanoETXexpress-SP is suitable for defense/aerospace and industrial applications, among others.

www.kontron.com

KONTRON

CD-ROM size NAS controller



VIA Technologies' NAS 7800 is a CD-ROM size board for storage servers with C7, SATA, CompactFlash, USB 2.0, and GigaLAN. The specialized segment board is targeted at SME Network Attached Storage (NAS) applications. It has integrated VIA UniChrom Pro graphics with 2D/3D and MPEG-2 video accelerations. It supports one VIA VT6130 PCIe GbE controller, one CompactFlash Type I slot, and one 32-bit MiniPCI slot for NAS 7800-15LST. Four SATA 3 Gbps (for NAS 7800-15T) or 8 SATA 3 Gbps (for NAS 7800-15LST) are also supported, in addition to four USB 2.0 ports and 12V DC-in (optional). NAS 7800 also includes an onboard Trusted Platform Module (TPM).

www.via.com.tw

VIA TECHNOLOGIES, INC.

Lightweight embedded computer

Ballard's (Avionics BusBox) AB1000 is a small, lightweight embedded computer with built-in interfaces for standard peripherals and various avionics databuses. Under the direction of its application-specific software, the AB1000 can autonomously perform tasks that involve receiving information from some interfaces and processing and mapping the information into other interfaces. It supports controls (Serial, Ethernet, and USB) and avionics databus (MIL-STD-1553, ARINC 429/708/717) interfaces. The computer is powered by a PowerPC 405GPr processor at 266 MHz and offers 64 MB SDRAM, 16 MB flash, and up to 8 Gb CF. A Software Development Kit (SDK) allows users to develop their applications using the included BTIDriver API. Consuming under 10 W, the computer can be used as a tethered I/O interface or programmed directly as a stand-alone device.

www.ballardtech.com

BALLARD TECHNOLOGY, INC.

Freescale Semiconductor's 8640D rekindles SBC power

By Duncan Young

Continued customer demand for more functionality and performance in the same or smaller space envelope, consuming less power, drives every new generation of SBC and DSP engine to stretch the limits of power dissipation in the highly competitive 6U VMEbus, VXS, and VPX rugged embedded computing market. Advanced semiconductor processing and packaging technology now offer COTS vendors the possibility to pack in more functionality and compute performance than can be adequately cooled, introducing the need for trade-offs to be made in some aspects of a product's characteristics.

The rugged, embedded mission-critical market still exhibits strong customer preference for Power Architecture devices and the VMEbus. This is the market's comfort zone with big investment by both vendors and their customers in applications development, system integration, tools, and hardware capability. Many of these customers are looking for the next generation of SBCs but are not yet ready for the complexity of migration to VPX, not necessarily needing more I/O capability or high-speed serial fabrics. The case for other processor architectures is often debated, and Intel's Core 2 Duo line of embedded processors, including the T7400 at up to 2 GHz, is certainly competitive in performance and power dissipation (between 20 W and 40 W). They also offer better integration with graphics. However, it is the application type that differentiates the processor choice. Intel will be selected for Man Machine Interface (MMI) applications and for network-centric, client/server architectures making use of off-the-shelf software solutions hosted on Solaris, Linux, or Windows. Power Architecture still dominates hard real-time, mission-critical applications, which are often custom developed to a specific platform type and must be robust and verifiable. Most of these applications are based on Wind River's VxWorks, LynuxWorks' LynxOS, or Green Hills' INTEGRITY.

The Freescale Semiconductor 8641D is the high-performance processor device of choice for this latter class of application. Vendors offer the 8641D on both SBC and DSP products with as many as four dual-core devices per 6U module already available. However, because of the potential to exceed the module's cooling capability, it might be necessary to push and pull each end-user's application parameters to best effect. This can be done by using single-core devices, reducing clock rates, restricting PMC/XMC additions, limiting the operating temperature range, or using the wider 1-inch pitch of VPX to gain extra cooling capacity, for example.

The 8641D was designed for the next generation of serial fabric-based architectures offering integrated 1 GbE, Serial RapidIO, and PCI Express (PCIe) as replacements for parallel data paths such as PCI, PCI-X, and even the VMEbus backplane. While providing this wealth of high-speed serial capability neatly targeted to either VXS or the newer VPX standards, the 8641D, by virtue of its e600 processing cores, also presents an opportunity to upgrade existing VMEbus SBCs. The majority of these SBCs use G4 (7447, 7457) Power Architecture devices and a Marvell Discovery bridge to provide the parallel PCI and PCI-X buses that provide connectivity to multiple I/O devices, the VMEbus and, in general, two PMC sites. From a user's perspective, changing from an existing SBC's PCI/PCI-X to the 8641's PCIe will be transparent, allowing easy migration of applications from one generation to the next.

A number of VMEbus SBCs have also been offered with two G4 devices, using the Discovery's versatile crossbar switching to provide links between processors and shared peripheral or I/O devices. This produces an innovative architecture configurable with one or two processor devices that can be loosely or tightly coupled as required by the application. To upgrade these dual-processor SBCs to dual 8641D devices, each potentially dissipating 30 W, pushes the power envelope of VMEbus and brings with it the need yet again to consider some application-dependent restrictions or performance limits. The newly introduced low-power Freescale Semiconductor 8640D goes a long way toward resolving this dilemma by offering comparable performance to the 8641D, yet dissipating 25 percent less power. The VG6 dual-processor SBC from GE Fanuc Intelligent Platforms shown in Figure 1 supports either dual 8641D or dual 8640D processors plus two PMC sites, being customizable for performance, functionality, or power dissipation to suit a broad spectrum of end-use applications.

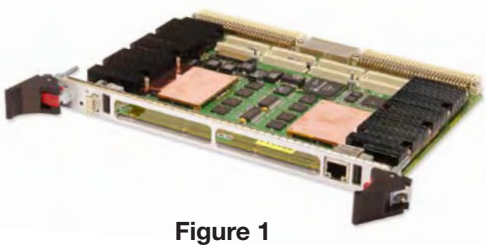


Figure 1

The 8640D provides the boost needed for the next generation of VMEbus SBCs. In a dual-processor configuration, a quad-core SBC can be implemented that supports compatible I/O functionality plus PMC/XMC sites offering no-compromise power dissipation. VMEbus and Power Architecture still have a lot of life left in the marketplace, capable of offering that continuous, plug-in upgrade path when the next performance boost is required.

To learn more, e-mail Duncan Young at young.duncan1@btinternet.com.

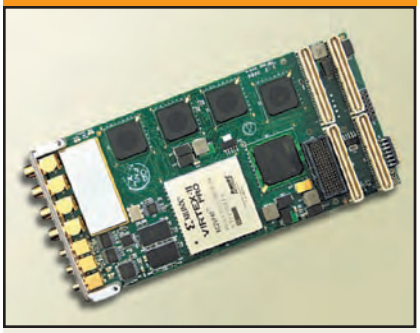
PowerPC AMC module

The XPedite6244 is a PowerPC processor AMC module with GbE, USB, and SATA support for MicroTCA/AdvancedTCA systems. It features a Freescale MPC7448 PowerPC processor running at up to 1.7 GHz and complies to AMC.0 and MicroTCA.0 (MicroTCA). The module supports up to 1 GB of 400 MHz DDR SDRAM and up to 64 MB of soldered NOR flash. Features include two SFP Ethernet ports, two RS-232 ports, and one USB port. Optional Ethernet AMC transport and SATA transport are also available. Green Hills INTEGRITY BSP, QNX Neutrino BSP, Linux LSP, and VxWorks BSP are supported.

www.xes-inc.com

EXTREME ENGINEERING SOLUTIONS

Wideband receiver PMC

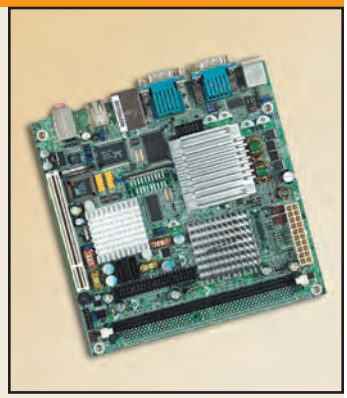


The DR PMC/XMC is a 16-channel wideband receiver PMC/XMC module featuring four LTC2255, 14-bit, 125 MSps converters. It includes a Virtex-II Pro FPGA providing 4 million gates, along with PCI 64/66 with P4 port to host card. Other features include 64 MB SDRAM, a low-jitter PLL clock source, advanced software and firmware demo programs, and a 10 Gbps full duplex XMC. DR PMC/XMC is suitable for applications such as Software-Defined Radio (SDR), signal identification, electronic warfare, and advanced radar.

www.innovative-dsp.com

INNOVATIVE INTEGRATION

Embedded Mini-ITX motherboard

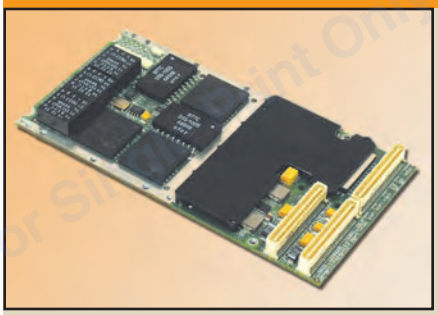


The G5G100-L10C is an embedded Mini-ITX motherboard utilizing the Mobile Intel 910GMLE Express chipset with Intel ICH6M I/O controller hub. It comes equipped with a 1 GHz Intel Celeron M Ultra Low Voltage 373 processor with 512 K cache, 400 MHz front-side bus, and integrated passive heat sink cooler. The G5G100-L10C consumes less than 17 W, making it suitable for applications with thermal or power restrictions. It features one 184-pin DDR 333 SDRAM DIMM socket accepting memory modules with capacities up to 1 GB. Additional features include one VGA port with integrated Intel GMA 900 graphics (2,048 x 1,536 @ 75 Hz), two Serial ATA ports, UltraDMA/100 IDE interface, eight USB 2.0/1.1 ports, four serial COM ports, and a GbE controller. Expansion is provided by one PCI slot.

www.itox.com

ITOX APPLIED COMPUTING

MIL-STD-1553 communications PMC



M705, a multi-I/O communications single-wide PMC with MIL-STD-1553B dual-redundant channels, has full support for BC/RT/MT operation modes. It includes 64 k x 16 shared DPRAM per channel, in addition to 16 ARINC-429 Receive channels, 8 ARINC-429 Transmit channels, and 6 serial channels. M705 offers complete UART operation and support for RS-232/RS-422/RS-485 physical interfacing. Two of the channels are configurable for modem hardware flow control. (Flow control signals support RS-232 only.) Other highlights include opto-isolated GND/OPEN discrete input channels, along with 32-bit @ 66 MHz PCI operation compliant with the PCI 2.2 specification. M705 also complies with the IEEE P1386 (Air-Cooled) and VITA 202001 (Conduction-Cooled) specifications. Front or rear I/O, hardware BIT capabilities, and drivers for VxWorks are also provided by M705, which implements military/space level ruggedization.

www.rugged.com

AITECH DEFENSE SYSTEMS

XMC graphics mezzanine card

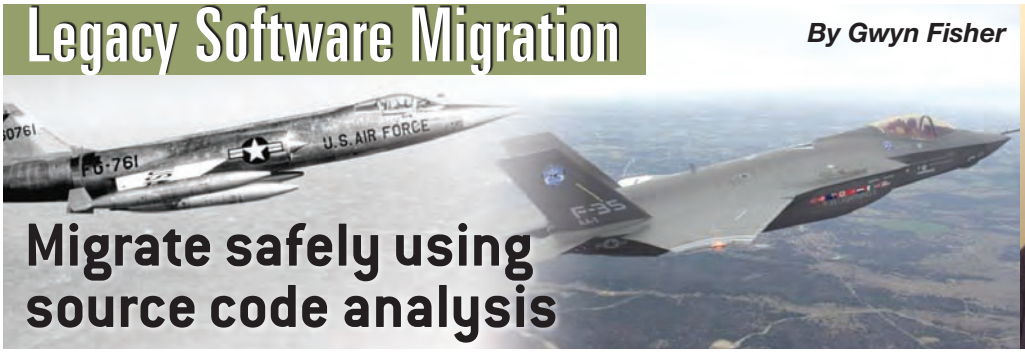
Quantum3D's Sentiris 5140 is an XMC mezzanine card and part of the Sentiris family of COTS graphics modules. Designed for use in general computing applications as well as air, ground, and maritime vehicles, the card includes the ATI Radeon HD 3650 and enables users to understand their environment in target recognition and "man-in-the-loop" training scenarios. Sentiris 5140 leverages Quantum3D's power-management technologies to reduce power consumption and heat dissipation. In addition, it meets the shock, vibration, temperature, and other requirements of MIL-STD-810F. The card ushers in a new era of General-Purpose Computing on Graphics Processing Units (GPGPU), enabling computation in addition to visualization. Sentiris 5140 is supported on x86 architectures running Windows XP Pro, Windows XP Embedded, and Linux operating systems.

www.quantum3d.com

QUANTUM3D

Legacy Software Migration

By Gwyn Fisher



Migrate safely using source code analysis

What can developers of military and avionics software systems do to take advantage of software reuse while ensuring that software is as bug-free and secure as possible?

It's not exactly a national security secret that software gets used and reused within the military and aerospace industries across different programs. This is a tried and true approach to software development. The GAO's March 2004 report to the U.S. Senate estimates software reuse at up to 70 percent on some projects, which presents significant opportunities in terms of cost savings and efficiencies. However, migrating this quantity of software is not without risk, particularly when destined for safety- or mission-critical software applications. So, the question is this: What can developers of military and avionics software systems do to take advantage of software reuse while ensuring that software is as bug-free and secure as possible?

Migrating software for use on new systems and combining with newly developed code present huge challenges for mission-critical systems. First and foremost are the size and scope of software systems today. The U.S. Army's Future Combat Systems (FCS) is estimated to deliver more than 60 million lines of software code in the end-product. Avionics software on the latest commercial jets runs into the many millions of lines of code; the software that runs the Boeing 787 approaches 7 million lines of code, triple that of the 777. To properly test software projects of this size, which have essentially an unlimited number of code paths to consider, is not trivial, especially when designed for use in a mission- and safety-critical context.

Added to this migration challenge is the fact that even though the code is being reused and would likely be considered stable after years of field operation, it is often operating in a new context or environment. This provides the possibility of formerly latent bugs turning into active, critical bugs and formerly safe coding practices becoming high-risk security vulnerabilities. This is not a theoretical discussion. This exact issue happened to the European Space Agency (ESA) with the launch of the Ariane 5 spacecraft, which reused code from its predecessor, Ariane 4. The code operated safely within the older craft, but the execution context changed, changing a "theoretical" or latent bug in the Ariane 4 into a critical bug that caused the crash of the Ariane 5. The same is true with security vulnerabilities: Coding practices from years ago in non-networked systems can become extremely high-risk vulnerabilities when deployed in a modern software context where systems are networked in a secure, mission-critical environment.

Software risk is well known to professionals in the industry, with the civilian aerospace software industry subject to the DO-178B regulations governing software development and verification requirements. These types of guidelines exist in many industries where safety requirements are paramount for software being developed. The challenge for software development professionals in these industries is finding the right mix of tools and processes that will address the unique challenges of reusing large amounts of code while being able to scale to the size and scope of mission-critical systems.

A growing trend in mission-critical software development is the adoption of Source Code Analysis (SCA) as a technology to augment (or even replace) traditional source code verification techniques such as peer code reviews, which aren't able to scale. SCA is a bug-detection technology that requires no test cases, is fully automated, and allows developers to inspect their source code extremely early in the development life cycle, ensuring that bugs aren't propagated downstream causing unwanted quality and efficiency headaches. The underlying technology associated with SCA is called *static analysis*, and the current generation of technology solutions is capable of providing sophisticated, fast, and accurate analysis that locates and describes areas of weakness in source code, including memory and resource management, program data management, buffer overflows, unvalidated user input, vulnerable coding practices, and concurrency violations, along with a variety of longer-term maintenance issues.

SCA is distinct from traditional dynamic analysis techniques, such as unit or penetration tests, because the work is performed at build time using only the source code of the program or module in question. The results reported are therefore generated from a complete view of every possible execution path, rather than some aspect of a limited, observed runtime behavior. This is particularly valuable in a legacy migration context where SCA can inspect hard-to-test areas such as error handling routines. SCA will also report on "potential" issues so that senior developers can ensure that changes in runtime context through reuse haven't created new sources of errors. When combined with existing testing and software validation techniques, SCA provides a scalable, efficient solution to large-scale verification of source code.

As the complexity of software explodes and its mission-critical nature continues to increase, the future of software testing and validation lies in continued automation. New forms of validation will extend the depth and breadth of technologies such as SCA and will combine them with other forms of software testing to deliver technology that creates innovative, comprehensive approaches to software validation.

***Gwyn Fisher** is Chief Technology Officer at Klocwork and has more than 20 years of global technology experience. He can be contacted at gwyn@klocwork.com.*

3U PXI module

The XJTAG 3U PXI module provides a high-speed interface to the boundary scan chain. The PXI card enables users of PXI chassis to leverage the ability to debug, test, and program complex ball grid array populated printed circuit boards and systems from within an integrated PXI test platform. The module provides enhanced boundary scan software to improve integration with National Instruments' LabVIEW graphical programming environment. PXI system users running LabVIEW software also get the added advantage of a full set of Virtual Instruments to interface to the XJTAG system.

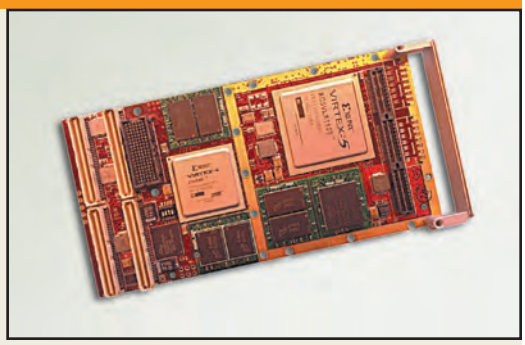
www.xjtag.com **XJTAG**

COM Express PC module

The SMX945, a Smart COM Express compliant PC module, is a small form factor, high-reliability, high-performance CPU module suitable for narrow space applications and harsh ambient conditions. It provides fanless, high dual-CPU core performance for video processing and video streaming applications. The proficient cooling feature ensures "perfect" thermal connection to a heat sink or enclosure. The SMX945 is compliant to PICMG COM Express with an Intel Celeron M, Core Duo processor, i945GM and ICH7-M chipset, 667 MHz FSB.

www.digitallogic.com
DIGITAL-LOGIC AG

Data acquisition PMC-X/XMC module



The FM486 is a high-performance PMC-X/XMC module dedicated to data acquisition, processing, and communication applications with complex requirements. High-speed DSP processing is executed via Xilinx Virtex-4 (FX20 or FX60) or Virtex-5 (SX95T or LX110T) FPGAs featuring off-the-shelf IP cores. In addition, memory includes 4x 64M x 16 DDR3 SDRAM devices (512 MB); 1x 2M x 18 QDR2+ SRAM devices (4 MB); up to 1x 64M x 32 DDR2 SDRAM devices (256 MB); and a 512 Mb flash device. PCI interfacing includes PCI-X 64-bit 133 MHz, 3.3 V; PCI 64/32-bit 66 MHz, 3.3 V; and PCI 64/32-bit 33 MHz, 3.3 V. Meanwhile, FM486 has PMC connector Pn4 64 user I/Os, 32 LVDS pairs or 64-bit single ended, and front-panel I/O daughtercards. Conduction cooling is optional.

www.4dsp.com **4DSP**

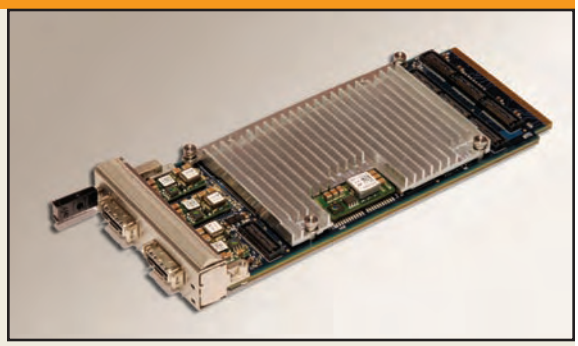
C development tools for Luminary MCU

code_red™

The Red Suite 1.5 comprises Eclipse-based C development tools offering advanced runtime tracing using serial wire-viewing capability in the Luminary Micro Stellaris microcontroller family, a nonstopping technology that gathers information nonintrusively as the target code executes. The suite adds support for project wizards, USB registers, and DMA controllers in the Stellaris family, giving better views into microcontroller and peripheral activities as well as enabling faster code writing and debugging. The tool also includes a FreeRTOS.org project wizard, which the company claims can generate a project skeleton in just four mouse clicks.

www.code-red-tech.com **CODE RED**

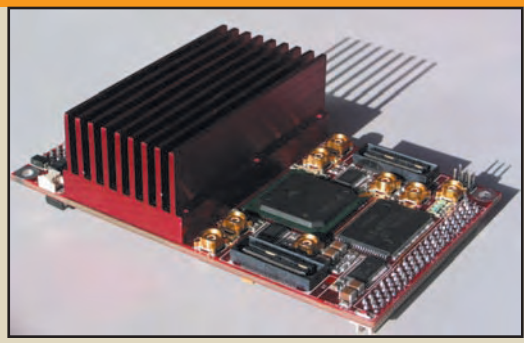
High-performance AdvancedMC DSP module



The AMC-D1F1-1200 is an AdvancedMC module that offers a compact, high-performance DSP/FPGA signal processing solution for AdvancedTCA and MicroTCA systems. It is powered by a Texas Instruments TMS320C6455 digital signal processor running at 1.2 GHz and a Xilinx Virtex-4 FX100 FPGA. The module is optimized for applications requiring high-end signal I/O bandwidth in a compact mid-height AdvancedMC form factor, such as wireless baseband, image processing, defense, and aerospace. It provides more than 256 MB of onboard memory. In addition, the FPGA is directly connected to the DSP via a high-bandwidth, low-latency 64-bit, 150 MHz local (EMIF) bus to facilitate coprocessing. Processor elements are interconnected by a 10 Gbps Serial RapidIO infrastructure with external connectivity to an AMC.4 backplane interface and front-panel connector.

www.commagility.com **COMMAGILITY**

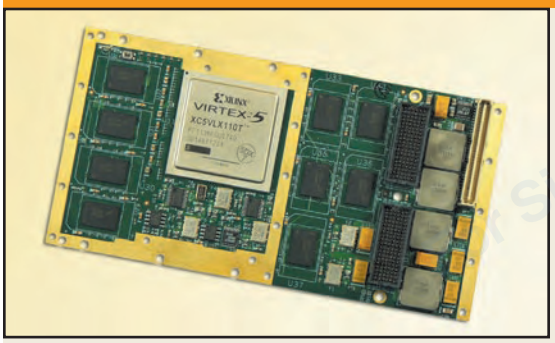
TIM-compatible DSP board



The SMT370-I is a TIM standard-compatible DSP board. It offers two 14-bit ADCs (AD6645) sampling up to 105 MHz, AC coupled, along with dual 16-bit TxDAC (AAD9777) sampling up to 400 MHz (interpolation), AC coupled. The single-width module includes two Sundance High-Speed Bus (SHB) connectors and two 20 MBps communication ports, along with a low-jitter system clock. Powered by a Xilinx Virtex-II FPGA (XC2V1000-6), the SMT370-I provides 50Ω analog inputs and outputs, external triggers and clocks via MMBX (HUBER+SUHNER) connectors, and user-defined pins for external connections.

www.sundance.com **SUNDANCE**

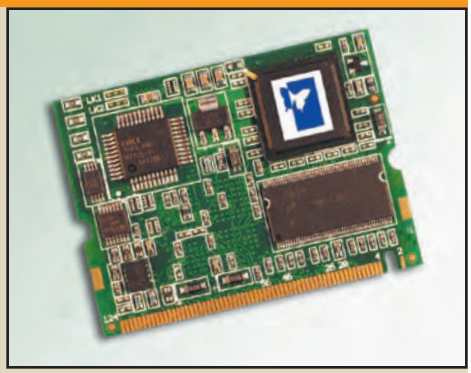
Buffer memory XMC



The MM-6171 is a buffer memory XMC with support for Serial RapidIO x4 or PCIe x8. Equipped with 2-4 GB of DDR2 SDRAM, the card provides high-speed buffering capabilities for DSP systems. The DDR2 SDRAM provides superior performance with low latency, while the bus interface with its full-featured DMA engine allows transactions to occur without host intervention. The VITA 42 compliant card interfaces to the host through the P15 connector. Four to eight high-speed serial links running at up to 3.125 GHz provide a high-speed full duplex interface. Connecting these high-speed signals to the memory arrays is a Xilinx Virtex-5 LX50T FPGA. Meanwhile, the DDR2 arrays provide more than 3 GBps of data bandwidth. VxWorks 6.x and Linux 2.6.x are supported, and rugged convection- and conduction-cooled versions are available.

www.vmetro.com **VMETRO**

microMPEG4 encoder/decoder



The microMPEG4 is a four-channel MPEG4 codec on a single Type III MiniPCI module. Utilizing the 32-bit PCI architecture, the device allows high-quality, real-time video and audio capture and compression from 1, 2, or 4 concurrent PAL or NTSC video sources to disk while at the same time providing an additional path for incoming video to be previewed on the host screen. The codec can also decompress and play back recordings from storage to display. microMPEG4 is supported by a suite of drivers for Windows 2000/XP, Linux, and QNX.

www.ampltd.com **ADVANCED MICRO PERIPHERALS, LTD.**

CompactRIO 1553 module

Averna's model 71553 is a CompactRIO module featuring dual-redundant MIL-STD-1553, an integrated BC/RT/BM architecture, and hot-swappable operation. It provides transformer or direct-coupled 1553 integration and supports 1553A/B Notice 2 protocol and LabVIEW functions. Features include four multicolor status LEDs, a DSUB 15-pin interface connector, and support for 9-35 VDC dual-input power. The small-sized module provides extreme ruggedness and flexibility and integrates graphical programming tools for rapid development. 71553's operating voltage ranges from +9 to +35 V, while its operating temperature is -40 °C to +70 °C.

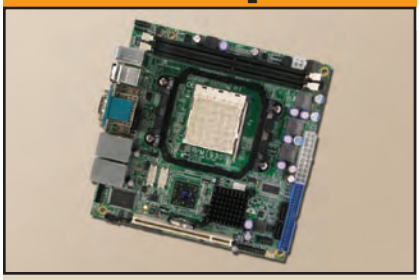
www.averna.com **AVERNA**

LVDT/RVDT-to-digital converter

The 73LD4 is a six-channel LVDT/RVDT-to-digital converter on a PC/104 card. Each channel has 16-bit resolution, 0.025 percent full scale accuracy, and a tracking rate to 150 strokes per second. Accurate digital velocity output, incremental encoder (A+B) outputs, and wraparound self-test are also provided. 73LD4 offers 16 programmable TTL digital input/output channels, a latch feature for reading all measurement channels simultaneously, and an optional programmable excitation reference supply.

www.naii.com
NORTH ATLANTIC INDUSTRIES

Mini-ITX single board computer

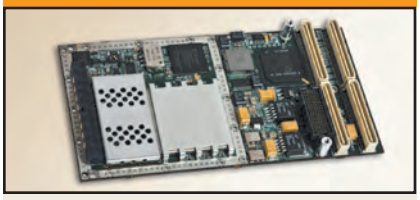


The MI935 Mini-ITX form factor SBC supports Intel's Core 2 Quad/Core 2 Duo/Celeron 400 sequence processors (Conroe-L) and Intel's latest Q35 Express chipset with a full 1,333 MHz FSB. The notebook computer-sized SBC measures 6.7" x 6.7" (170 mm x 170 mm) and provides two DDR2 DIMM slots. MI935 can support up to 4 GB of DRAM and features a 10/100BASE-T Ethernet port, integrated VGA, 8x USB 2.0, 2x SATA II, 1x eSATA, and 2x COM ports. The MI935 is a good fit for full-featured but small-sized PC-based military systems.

www.ibase-i.com.tw

IBASE TECHNOLOGY

XMC/PMC digital transmitter

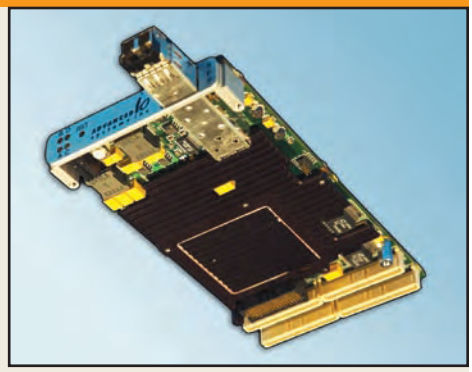


The ICS-8560 is an XMC/PMC form factor digital transmitter module intended for Software-Defined Radio (SDR) applications. It features two AC-coupled analog outputs, 16-bit resolution (Analog Devices AD9726), FS ≤ 200 MHz (Single Data Rate Mode), and FS ≤ 400 MHz (Double Data Rate Mode). It includes a Xilinx Virtex-4 FX60 or FC100 FPGA with multiple IP cores (including SDR 200 MHz, DDR 400 MHz), along with a Hardware Development Kit (HDK). ICS-8560 also comprises an eight-connector Samtec GRF1-J connector (Ruggedization Levels 1, 2, and 3) and eight individual MMCX connectors (Ruggedization Levels 4 and 5). Serving as companion to V4DSP 6U VME FPGAs and PowerPC processors, ICS-8560 supports VxWorks, Linux, and Windows software drivers.

www.gefanuc.com/embedded

GE FANUC INTELLIGENT PLATFORMS, INC.

Intelligent 10 GbE XMC/PMC module

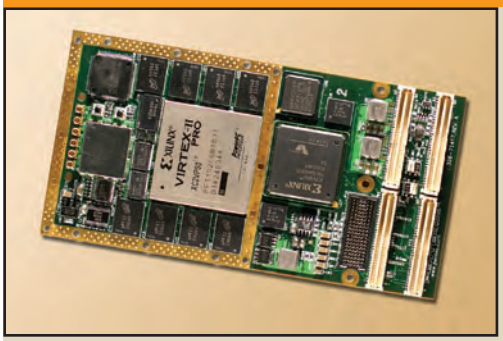


AdvancedIO Systems' V1021 is an intelligent XMC/PMC module that provides 10 GbE connectivity for demanding real-time applications. It enables use of 10 GbE as a high-performance fabric, and is designed per VITA 42.3. Features include a Xilinx Virtex-II Pro FPGA and standard 10 GbE SFP+ optical interface. The V1021 also has PCI Express x4 and PCI-X 133 MHz interfaces, and udpXG protocol offload or streamXG direct data streaming (optional). The high-speed interface with carrier board additionally presents two options: PCIe 4x (four-lane), nominal 1 GBps full duplex; and PCI-X 133 MHz, nominal 1,064 MBps simplex. It supports software environments including VxWorks, Linux, and standard Sockets API.

www.advancedio.com

ADVANCEDIO SYSTEMS

Software radio transceiver



Model 7141 is a dual-channel software radio transceiver with Xilinx Virtex-II Pro FPGA and 512 MB of DDR SDRAM. The transceiver includes a PMC/XMC suitable for connection to HF or IF ports in a communications system and is VITA 42.0 XMC compatible with switched fabric interfaces. It provides two 125 MHz 14-bit A/Ds and two 500 MHz 16-bit D/As, four digital downconverters, and one digital upconverter. Other features include dual timing buses for independent input and output clock rates, LVDS clock/sync bus for multiple module synchronization, and optional factory-installed IP cores. Ruggedized and conduction-cooled versions are available.

www.pentek.com

PENTEK, INC.

Synchronous WAN communications module

The AMC335 is a multipurpose, intelligent synchronous WAN communications module for AdvancedTCA and MicroTCA systems. It complies with the AMC.0 R2.0, AMC.1 R1.0, and AMC.2 R1.0 specifications and provides four high-speed channels capable of sustaining 2 Mbps per port. Powered by a Freescale MPC8270 PowerQUICC II processor, the AMC335 features 128 MB of dedicated processor SDRAM memory and handles extensive onboard traffic and protocol requirements. Application flash (32 MB) is also offered, along with NexusWare WAN protocol software: Radar Receiver, TADIL-B, HDLC, X.25, Frame Relay, ASYNC, and NexusWare CGL OS and development environment. Broad operating system support includes Solaris, Windows, and Linux.

www.pt.com

PERFORMANCE TECHNOLOGIES